

4K SPI[™] Bus Serial EEPROM

Device Selection Table

Part Number	Vcc Range	Max. Clock Frequency	Temp. Ranges
25AA040	1.8-5.5V	1 MHz	I
25LC040	2.5-5.5V	2 MHz	I
25C040	4.5-5.5V	3 MHz	I,E

Features

Low-power CMOS technology

- Write current: 3 mA typical

Read current: 500 μA typical
Standby current: 500 nA typical

• 512 x 8-bit organization

• 16 byte page

· Write cycle time: 5 ms max.

· Self-timed ERASE and WRITE cycles

· Block write protection

- Protect none, 1/4, 1/2 or all of array

· Built-in write protection

- Power on/off data protection circuitry

- Write enable latch

- Write-protect pin

· Sequential read

· High reliability

- Endurance: 1M cycles

- Data retention: > 200 years

- ESD protection: > 4000V

· 8-pin PDIP, SOIC, and TSSOP packages

• Temperature ranges supported:

- Industrial (I): -40°C to +85°C - Automotive (E) (25C040): -40°C to +125°C

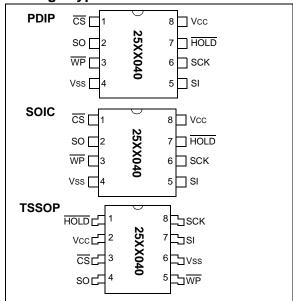
Description

The Microchip Technology Inc. 25AA040/25LC040/25C040 (25XX040*) is a 4 Kbit serial Electrically Erasable PROM. The memory is accessed via a simple Serial Peripheral Interface (SPITM) compatible serial bus. The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a Chip Select ($\overline{\text{CS}}$) input.

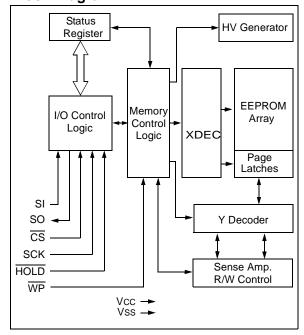
*25XX040 is used in this document as a generic part number for the 25AA040/25LC040/25C040 devices. SPI is a trademark of Motorola Corporation.

Communication to the device can be paused via the hold pin ($\overline{\text{HOLD}}$). While the device is paused, transitions on its inputs will be ignored, with the exception of Chip Select, allowing the host to service higher priority interrupts. Also, write operations to the device can be disabled via the write-protect pin ($\overline{\text{WP}}$).

Package Types



Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

Vcc	7.0V
All inputs and outputs w.r.t. Vss	0.6V to Vcc+1.0V
Storage temperature	65°C to 150°C
Ambient temperature under bias	65°C to 125°C
ESD protection on all pins	4 KV

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability

TABLE 1-1: DC CHARACTERISTICS

DC CHA	DC CHARACTERISTICS			Industrial (I): TA = -40°C to +85°C				
Param. No.	Sym.	Characteristic Min. Max. Units		Test Conditions				
D001	VIH1	High-level input	2.0	Vcc+1	V	Vcc ≥ 2.7V (Note)		
D002	VIH2	voltage	0.7 Vcc	Vcc+1	V	VCC< 2.7V (Note)		
D003	VIL1	Low-level input	-0.3	0.8	V	Vcc ≥ 2.7V (Note)		
D004	VIL2	voltage	-0.3	0.3 Vcc	V	Vcc < 2.7V (Note)		
D005	Vol	Low-level output	_	0.4	V	IOL = 2.1 mA		
D006	Vol	voltage	_	0.2	V	IOL = 1.0 mA, VCC < 2.5V		
D007	Voн	High-level output voltage	Vcc -0.5	_	V	ΙΟΗ =-400 μΑ		
D008	ILI	Input leakage current	_	±1	μΑ	CS = Vcc, Vin = Vss to Vcc		
D009	ILO	Output leakage current	_	±1	μА	CS = Vcc, Vout = Vss to Vcc		
D010	CINT	Internal Capacitance (all inputs and outputs)	_	7	pF	TA = 25°C, CLK = 1.0 MHz, VCC = 5.0V (Note)		
D011	Icc Read	Operating Current	_	1 500	mA μA	VCC = 5.5V; FCLK = 3.0 MHz; SO = Open VCC = 2.5V; FCLK = 2.0 MHz; SO = Open		
D012	Icc Write		_	5	mA	Vcc = 5.5V		
			_	3	mA	VCC = 2.5V		
D013	Iccs	Standby Current		5 1	μA μA	$\overline{\text{CS}}$ = Vcc = 5.5V, Inputs tied to Vcc or Vss $\overline{\text{CS}}$ = Vcc = 2.5V, Inputs tied to Vcc or Vss		

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-2: AC CHARACTERISTICS

AC CHA	RACTER	ISTICS	Industrial (I): $TA = -40^{\circ}C$ to $+85^{\circ}C$ Automotive (E): $TA = -40^{\circ}C$ to $+125^{\circ}C$			
Param No.	Sym.	Characteristic	Min.	Max.	Units	Test Conditions
1	FCLK	Clock Frequency	_	3	MHz	Vcc = 4.5V to 5.5V
		, ,	_	2	MHz	VCC = 2.5V to 4.5V
			_	1	MHz	VCC = 1.8V to 2.5V
2	Tcss	CS Setup Time	100	_	ns	VCC = 4.5V to 5.5V
			250	_	ns	VCC = 2.5V to 4.5V
			500	_	ns	Vcc = 1.8V to 2.5V
3	TCSH	CS Hold Time	150	_	ns	VCC = 4.5V to 5.5V
			250	_	ns	VCC = 2.5V to 4.5V
		<u> </u>	475		ns	VCC = 1.8V to 2.5V
4	TCSD	CS Disable Time	500		ns	_
5	Tsu	Data Setup Time	30	_	ns	VCC = 4.5V to 5.5V
			50	_	ns	VCC = 2.5V to 4.5V
			50	_	ns	VCC = 1.8V to 2.5V
6	THD	Data Hold Time	50	_	ns	VCC = 4.5V to 5.5V
			100	_	ns	Vcc = 2.5V to 4.5V
			100	_	ns	VCC = 1.8V to 2.5V
7	TR	CLK Rise Time	_	2	μs	(Note 1)
8	TF	CLK Fall Time	_	2	μs	(Note 1)
9	Тні	Clock High Time	150	_	ns	VCC = 4.5V to 5.5V
			230	_	ns	VCC = 2.5V to 4.5V
			475	_	ns	VCC = 1.8V to 2.5V
10	TLO	Clock Low Time	150	_	ns	VCC = 4.5V to 5.5V
			230	_	ns	VCC = 2.5V to 4.5V
			475	_	ns	VCC = 1.8V to 2.5V
11	TCLD	Clock Delay Time	50	_	ns	_
12	TCLE	Clock Enable Time	50	_	ns	_
13	Tv	Output Valid from Clock Low	_	150	ns	VCC = 4.5V to 5.5V
			_	230	ns	VCC = 2.5V to 4.5V
			_	475	ns	VCC = 1.8V to 2.5V
14	Тно	Output Hold Time	0	_	ns	(Note 1)
15	Tois	Output Disable Time	_	200	ns	Vcc = 4.5V to 5.5V (Note 1)
			_	250	ns	VCC = 2.5V to 4.5V (Note 1)
			_	500	ns	VCC = 1.8V to 2.5V (Note 1)
16	THS	HOLD Setup Time	100	_	ns	VCC = 4.5V to 5.5V
			100	_	ns	VCC = 2.5V to 4.5V
			200	_	ns	VCC = 1.8V to 2.5V
17	Тнн	HOLD Hold Time	100		ns	VCC = 4.5V to 5.5V
			100	_	ns	VCC = 2.5V to 4.5V
			200		ns	VCC = 1.8V to 2.5V
18	THZ	HOLD Low to Output High-Z	100	_	ns	VCC = 4.5V to 5.5V (Note 1)
			150	_	ns	VCC = 2.5V to 4.5V (Note 1)
			200		ns	VCC = 1.8V to 2.5V (Note 1)
19	THV	HOLD High to Output Valid	100	-	ns	VCC = 4.5V to 5.5V
			150	-	ns	Vcc = 2.5V to 4.5V
			200		ns	VCC = 1.8V to 2.5V
20	Twc	Internal Write Cycle Time	_	5	ms	_
21	-	Endurance	1M		E/W	(Note 2)
					Cycles	

Note 1: This parameter is periodically sampled and not 100% tested.

^{2:} This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from our web site: www.microchip.com.

FIGURE 1-1: HOLD TIMING

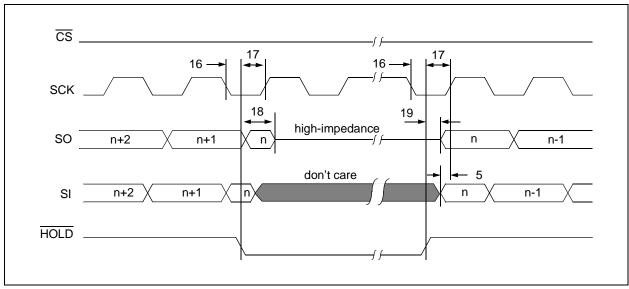


FIGURE 1-2: SERIAL INPUT TIMING

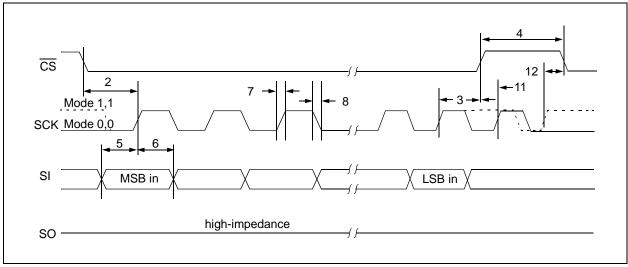


FIGURE 1-3: SERIAL OUTPUT TIMING

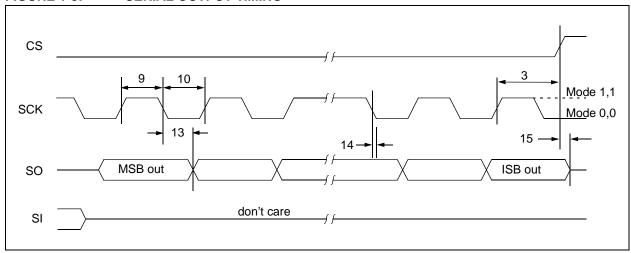
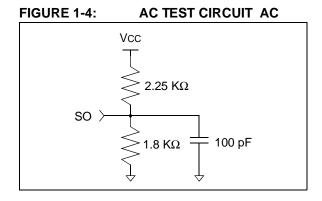


TABLE 1-3: AC TEST CONDITIONS

AC Waveform:					
VLO = 0.2V	_				
VHI = VCC - 0.2V	(Note 1)				
VHI = 4.0V	(Note 2)				
Timing Measurement Reference Level					
Input	0.5 Vcc				
Output	0.5 Vcc				

Note 1: For VCC ≤ 4.0V **2:** For VCC > 4.0V



2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Name	PDIP	SOIC	TSSOP	Description
CS	1	1	3	Chip Select Input
so	2	2	4 Serial Data Outp	
WP	3	3	5	Write-Protect Pin
Vss	4	4	6	Ground
SI	5	5	7	Serial Data Input
SCK	6	6	8	Serial Clock Input
HOLD	7	7	1	Hold Input
Vcc	8	8	2	Supply Voltage

2.1 Chip Select (CS)

A low level on this pin selects the device. A high level deselects the device and forces it into Standby mode. However, a programming cycle which is already initiated or in progress will be completed, regardless of the $\overline{\text{CS}}$ input signal. If $\overline{\text{CS}}$ is brought high during a program cycle, the device will go in Standby mode as soon as the programming cycle is complete. When the device is deselected, SO goes into the high-impedance state, allowing multiple parts to share the same SPI bus. A low-to-high transition on $\overline{\text{CS}}$ after a valid write sequence initiates an internal write cycle. After power-up, a low level on $\overline{\text{CS}}$ is required prior to any sequence being initiated.

2.2 Serial Output (SO)

The SO pin is used to transfer data out of the 25XX040. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

2.3 Write-Protect (WP)

This pin is a hardware write-protect input pin. When \overline{WP} is low, all writes to the array or Status register are disabled, but any other operation functions normally. When \overline{WP} is high, all functions, including nonvolatile writes operate normally. \overline{WP} going low at any time will reset the write enable latch and inhibit programming, except when an internal write has already begun. If an internal write cycle has already begun, \overline{WP} going low will have no effect on the write. See Table 3-2 for Write-Protect Functionality Matrix.

2.4 Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses and data. Data is latched on the rising edge of the serial clock.

2.5 Serial Clock (SCK)

The SCK is used to synchronize the communication between a master and the 25XX040. Instructions, addresses or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

2.6 Hold (HOLD)

The HOLD pin is used to suspend transmission to the 25XX040 while in the middle of a serial sequence without having to retransmit the entire sequence again at a later time. It must be held high any time this function is not being used. Once the device is selected and a serial sequence is underway, the HOLD pin may be pulled low to pause further serial communication without resetting the serial sequence. The HOLD pin must be brought low while SCK is low, otherwise the HOLD function will not be invoked until the next SCK high-tolow transition. The 25XX040 must remain selected during this sequence. The SI, SCK and SO pins are in a high-impedance state during the time the part is paused and transitions on these pins will be ignored. To resume serial communication, HOLD must be brought high while the SCK pin is low, otherwise serial communication will not resume. Lowering the HOLD line at any time will tri-state the SO line.

3.0 FUNCTIONAL DESCRIPTION

3.1 Principles of Operation

The 25XX040 is a 512 byte Serial EEPROM designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today's popular microcontroller families, including Microchip's PIC16C6X/7X microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly with the software.

The 25XX040 contains an 8-bit instruction register. The part is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The $\overline{\text{CS}}$ pin must be low and the $\overline{\text{HOLD}}$ pin must be high for the entire operation. The $\overline{\text{WP}}$ pin must be held high to allow writing to the memory array.

Table 3-1 contains a list of the possible instruction bytes and format for device operation. The Most Significant address bit (A8) is located in the instruction byte. All instructions, addresses, and data are transferred MSB first. LSB last.

Data is sampled on the first rising edge of SCK after $\overline{\text{CS}}$ goes low. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{\text{HOLD}}$ input and place the 25XX040 in 'HOLD' mode. After releasing the $\overline{\text{HOLD}}$ pin, operation will resume from the point when the $\overline{\text{HOLD}}$ was asserted.

3.2 Read Sequence

The part is selected by pulling $\overline{\text{CS}}$ low. The 8-bit read instruction with the A8 address bit is transmitted to the 25XX040 followed by the lower 8-bit address (A7 through A0). After the correct READ instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. The data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses. The internal address pointer is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (01FFh), the address counter rolls over to address 0000h allowing the read cycle to be continued indefinitely. The read operation is terminated by raising the $\overline{\text{CS}}$ pin (Figure 3-1).

3.3 Write Sequence

Prior to any attempt to write data to the 25XX040, the write enable latch must be set by issuing the WREN instruction (Figure 3-4). This is done by setting $\overline{\text{CS}}$ low and then clocking out the proper instruction into the 25XX040. After all eight bits of the instruction are transmitted, the $\overline{\text{CS}}$ must be brought high to set the write enable latch. If the write operation is initiated immediately after the WREN instruction without $\overline{\text{CS}}$ being brought high, the data will not be written to the array because the write enable latch will not have been properly set.

Once the write enable latch is set, the user may proceed by setting the $\overline{\text{CS}}$ low, issuing a WRITE instruction, followed by the address, and then the data to be written. Keep in mind that the Most Significant address bit (A8) is included in the instruction byte. Up to 16 bytes of data can be sent to the 25XX040 before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page. A page address begins with XXXX 0000 and ends with XXXX 1111. If the internal address counter reaches XXXX 1111 and the clock continues, the counter will roll back to the first address of the page and overwrite any data in the page that may have been written.

For the data to be actually written to the array, the $\overline{\text{CS}}$ must be brought high after the least significant bit (D0) of the n^{th} data byte has been clocked in. If $\overline{\text{CS}}$ is brought high at any other time, the write operation will not be completed. Refer to Figure 3-2 and Figure 3-3 for more detailed illustrations on the byte write sequence and the page write sequence respectively. While the write is in progress, the Status register may be read to check the status of the WIP, WEL, BP1 and BP0 bits (Figure 3-6). A read attempt of a memory array location will not be possible during a write cycle. When the write cycle is completed, the write enable latch is reset.

TABLE 3-1: INSTRUCTION SET

Instruction Name	Instruction Format	Description
READ	0000 A8011	Read data from memory array beginning at selected address
WRITE	0000 A8010	Write data to memory array beginning at selected address
WRDI	0000 0100	Reset the write enable latch (disable write operations)
WREN	0000 0110	Set the write enable latch (enable write operations)
RDSR	0000 0101	Read Status register
WRSR	0000 0001	Write Status register

Note: As is the 9th address bit necessary to fully address 512 bytes.

FIGURE 3-1: READ SEQUENCE

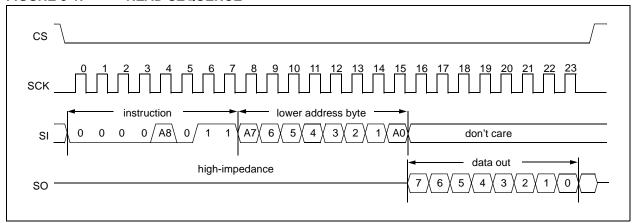


FIGURE 3-2: BYTE WRITE SEQUENCE

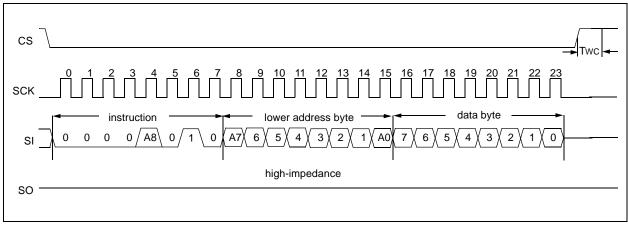
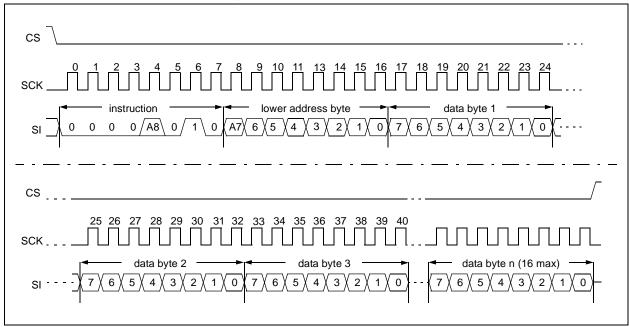


FIGURE 3-3: PAGE WRITE SEQUENCE



3.4 Write Enable (WREN) and Write Disable (WRDI)

The 25XX040 contains a write enable latch. See Table 3-3 for the Write-Protect Functionality Matrix. This latch must be set before any write operation will be completed internally. The WREN instruction will set the latch, and the WRDI will reset the latch.

The following is a list of conditions under which the write enable latch will be reset:

- Power-up
- WRDI instruction successfully executed
- WRSR instruction successfully executed
- WRITE instruction successfully executed
- WP line is low

FIGURE 3-4: WRITE ENABLE SEQUENCE

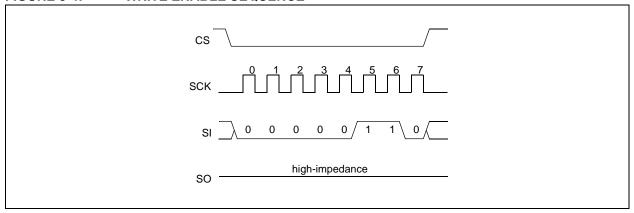
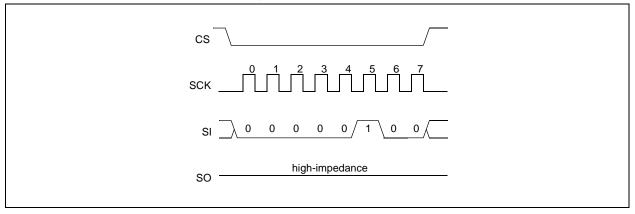


FIGURE 3-5: WRITE DISABLE SEQUENCE



3.5 Read Status Register (RDSR)

The RDSR instruction provides access to the Status register. The Status register may be read at any time, even during a write cycle. The Status register is formatted as follows:

7	6	5	4	3	2	1	0
Х	Х	Х	Х	BP1	BP0	WEL	WIP

The **Write-In-Process (WIP)** bit indicates whether the 25XX040 is busy with a write operation. When set to a '1', a write is in progress, when set to a '0', no write is in progress. This bit is read only.

The **Write Enable Latch (WEL)** bit indicates the status of the write enable latch. When set to a '1', the latch allows writes to the array, when set to a '0', the latch prohibits writes to the array. The state of this bit can always be updated via the WREN or WRDI commands regardless of the state of write protection on the Status register. This bit is read only.

The **Block Protection (BP0 and BP1)** bits indicate which blocks are currently write-protected. These bits are set by the user issuing the \mathtt{WRSR} instruction. These bits are nonvolatile.

See Figure 3-6 for RDSR timing sequence.

3.6 Write Status Register (WRSR)

The WRSR instruction allows the user to select one of four levels of protection for the array by writing to the appropriate bits in the Status register. The array is divided up into four segments. The user has the ability to write-protect none, one, two, or all four of the segments of the array. The partitioning is controlled as illustrated in Table 3-2.

See Figure 3-7 for WRSR timing sequence.

TABLE 3-2: ARRAY PROTECTION

BP1	BP0	Array Addresses Write-Protected
0	0	none
0	1	upper 1/4 (0180h - 01FFh)
1	0	upper 1/2 (0100h - 01FFh)
1	1	all (0000h - 01FFh)

FIGURE 3-6: READ STATUS REGISTER SEQUENCE

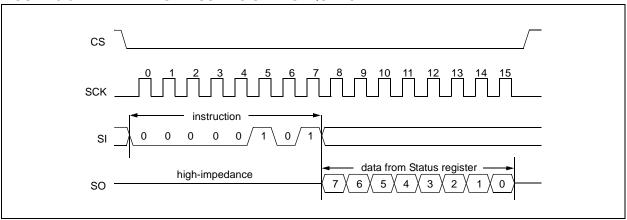
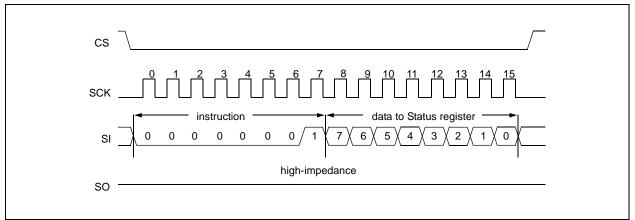


FIGURE 3-7: WRITE STATUS REGISTER SEQUENCE



3.7 Data Protection

The following protection has been implemented to prevent inadvertent writes to the array:

- The write enable latch is reset on power-up
- A write enable instruction must be issued to set the write enable latch
- After a byte write, page write or Status register write, the write enable latch is reset
- CS must be set high after the proper number of clock cycles to start an internal write cycle
- Access to the array during an internal write cycle is ignored and programming is continued

3.8 Power-On State

The 25XX040 powers on in the following state:

- The device is in low-power Standby mode (CS = 1)
- The write enable latch is reset
- SO is in high-impedance state
- A low level on $\overline{\text{CS}}$ is required to enter active state

TABLE 3-3: WRITE-PROTECT FUNCTIONALITY MATRIX

WP	WEL	Protected Blocks	Unprotected Blocks	Status Register
Low	Х	Protected	Protected	Protected
High	0	Protected	Protected	Protected
High	1	Protected	Writable	Writable

4.0 PACKAGING INFORMATION

4.1 Package Marking Information

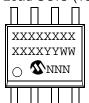




Example:



8-Lead SOIC (150 mil)







8-Lead TSSOP



Example:



Legend: XX...X Customer specific information*

Y Year code (last digit of calendar year)
YY Year code (last 2 digits of calendar year)
WW Week code (week of January 1 is week '01')

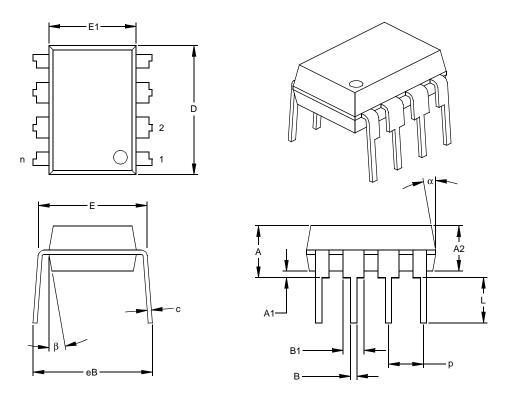
NNN Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters

for customer specific information.

* Standard PICmicro device marking consists of Microchip part number, year code, week code, and traceability code. For PICmicro device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

8-Lead Plastic Dual In-line (P) - 300 mil (PDIP)



	Units			INCHES*			MILLIMETERS		
Dimens	ion Limits	MIN	NOM	MAX	MIN	NOM	MAX		
Number of Pins	n		8			8			
Pitch	р		.100			2.54			
Top to Seating Plane	Α	.140	.155	.170	3.56	3.94	4.32		
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68		
Base to Seating Plane	A1	.015			0.38				
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26		
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60		
Overall Length	D	.360	.373	.385	9.14	9.46	9.78		
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43		
Lead Thickness	С	.008	.012	.015	0.20	0.29	0.38		
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78		
Lower Lead Width	В	.014	.018	.022	0.36	0.46	0.56		
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92		
Mold Draft Angle Top	α	5	10	15	5	10	15		
Mold Draft Angle Bottom	β	5	10	15	5	10	15		

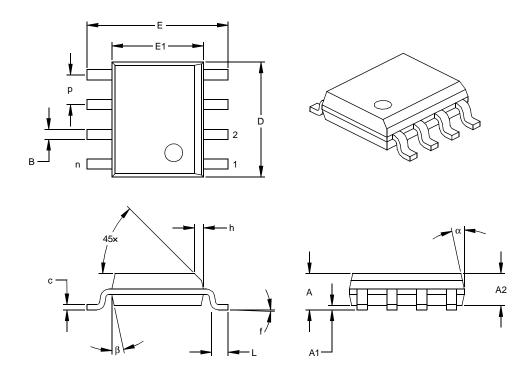
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-001

Drawing No. C04-018

^{*} Controlling Parameter § Significant Characteristic

8-Lead Plastic Small Outline (SN) - Narrow, 150 mil (SOIC)



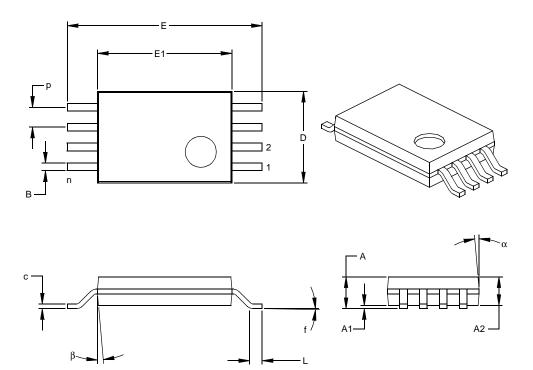
	Units	INCHES*			MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	р		.050			1.27	
Overall Height	Α	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	Е	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	f	0	4	8	0	4	8
Lead Thickness	С	.008	.009	.010	0.20	0.23	0.25
Lead Width	В	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed

.010" (0.254mm) per side. JEDEC Equivalent: MS-012 Drawing No. C04-057

^{*} Controlling Parameter § Significant Characteristic

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)



	Units	Jnits INCHES			MILLIMETERS*		
Dimens	ion Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	р		.026			0.65	
Overall Height	Α			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	f	0	4	8	0	4	8
Lead Thickness	С	.004	.006	.008	0.09	0.15	0.20
Lead Width	В	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

^{*} Controlling Parameter

Notes

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed

.005" (0.127mm) per side.
JEDEC Equivalent: MO-153
Drawing No. C04-086

[§] Significant Characteristic

APPENDIX A: REVISION HISTORY

Revision D

Corrections to Section 1.0, Electrical Characteristics.

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PART NO.	X	<u>/XX</u>	<u>xxx</u>	Exa	amples:
Device	Temperature Range	Package	Pattern	a) b)	25AA040-I/P: Industrial Temp., PDIP package 25AA040-I/SN: Industrial Temp., SOIC package
Device:	25AA040T: 25XX040X: 25AA040X: 25LC040: 25LC040X: 25LC040X: 25C040: 25C040T: 25C040X:	4096-bit 1.8V (Tape and Re 4096-bit 1.8V in alternate p T:4096-bit 1.8V in alternate p (ST only) 4096-bit 2.5V (Tape and Re 4096-bit 2.5V in alternate p (ST only) 4096-bit 5.0V (Tape and Re 4096-bit 5.0V (Tape and Re 4096-bit 5.0V in alternate p	/ SPI Serial EEPROM pinout (ST only) / SPI Serial EEPROM pinout Tape and Reel / SPI Serial EEPROM / SPI Serial EEPROM peel) / SPI Serial EEPROM pinout (ST only) / SPI Serial EEPROM pinout Tape and Reel / SPI Serial EEPROM pinout Tape and Reel / SPI Serial EEPROM / SPI Serial EEPROM / SPI Serial EEPROM	f) g) h) i) k)	25AA040T-I/SN: Tape and Reel, Industrial Temp., SOIC package 25AA040X-I/ST: Alternate Pinout, Industrial Temp., TSSOP package 25AA040XT-I/ST: Alternate Pinout, Tape and Reel, Industrial Temp., TSSOP package 25LC040-I/P: Industrial Temp., PDIP package 25LC040-I/SN: Industrial Temp., SOIC package 25LC040T-I/SN: Tape and Reel, Industrial Temp., SOIC package 25LC040X-I/ST: Alternate Pinout, Industrial Temp., TSSOP package 25LC040XT-I/ST: Alternate Pinout, Tape and Reel, Industrial Temp., TSSOP package 25LC040XT-I/ST: Alternate Pinout, Tape and Reel, Industrial Temp., TSSOP package 25C040-I/P: Industrial Temp., TSSOP package 25C040-I/P: Industrial Temp., PDIP package 25C040-I/SN: Industrial Temp., SOIC package
Temperature Range:		-40 °C to+85 ° 40 °C to+125		m)	25C040T-I/SN: Tape and Reel, Industrial Temp., SOIC package 25C040X-I/ST: Alternate Pinout, Industrial Temp., TSSOP package
Package:	P = SN = ST =	Plastic SOIC	300 mil body), 8-lead 3 (150 mil body), 8-lead 3 (150 mil body), 8-lead 3 (150 mm body), 8-lead	o) p) q) r) s) t)	25C040XT-I/ST: Alternate Pinout, Tape and Reel, Industrial Temp., TSSOP package 25C040-E/P: Extended Temp., PDIP package 25C040-E/SN: Extended Temp., SOIC package 25C040T-E/SN: Tape and Reel, Extended Temp., SOIC package 25C040X-E/ST: Alternate Pinout, Extended Temp., TSSOP package 25C040XT-E/ST: Alternate Pinout, Tape and Reel, Extended Temp., TSSOP package

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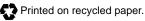
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