HM628128B Series

131,072-word × 8-bit High speed CMOS Static RAM

HITACHI

ADE-203-243B (Z)
Rev. 2.0
Mar. 20, 1995

Description

The Hitachi HM628128B is a CMOS static RAM organized 131,072-word × 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.8 µm Hi-CMOS shrink process technology. It offers low power standby power dissipation, therefore, it is suitable for battery backup systems. The device, packaged in a 525 mil SOP or a 8 mm × 20 mm TSOP or a 600 mil plastic DIP is available.

Features

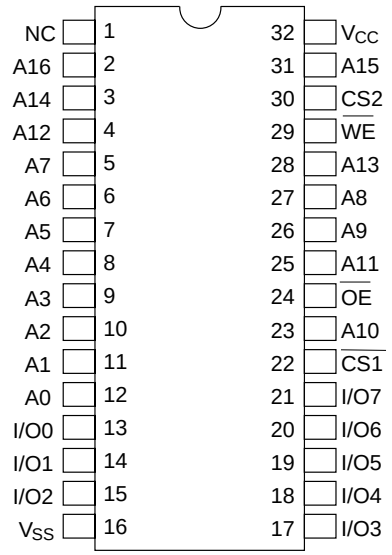
- High speed
  - — Fast access time: 70/85ns (max)
- Low power
  - — Standby: 10 µW (typ) (L/L-SL version)
  - — Operation: 50 mW/MHz (typ)
- Single 5 V supply
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- Common data input and output
  Three state output
- Directly TTL compatible
  All inputs and outputs
- Capability of battery backup operation (L/L-SL version)
  2 chip selection for battery backup

Ordering Information

Type No.	Access Time	Data Retention Current	Package
HM628128BLP-7	70 ns	50 µA	600-mil 32-pin plastic DIP (DP-32)
HM628128BLP-8	85 ns	50 µA	
HM628128BLP-7SL	70 ns	15 µA	
HM628128BLP-8SL	85 ns	15 µA	
HM628128BLFP-7	70 ns	50 µA	525-mil 32-pin plastic SOP (FP-32D)
HM628128BLFP-8	85 ns	50 µA	
HM628128BLFP-7SL	70 ns	15 µA	
HM628128BLFP-8SL	85 ns	15 µA	
HM628128BLT-7	70 ns	50 µA	Normal-bend type 32-pin plastic 8 mm × 20 mm TSOP (TFP-32D)
HM628128BLT-8	85 ns	50 µA	
HM628128BLT-7SL	70 ns	15 µA	
HM628128BLT-8SL	85 ns	15 µA	
HM628128BLR-7	70 ns	50 µA	Reverse-bend type 32-pin plastic 8 mm × 20 mm TSOP (TFP-32DR)
HM628128BLR-8	85 ns	50 µA	
HM628128BLR-7SL	70 ns	15 µA	
HM628128BLR-8SL	85 ns	15 µA	

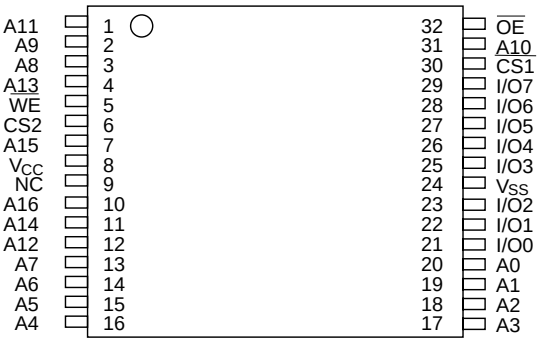
Pin Arrangement

HM628128BP/BFP Series



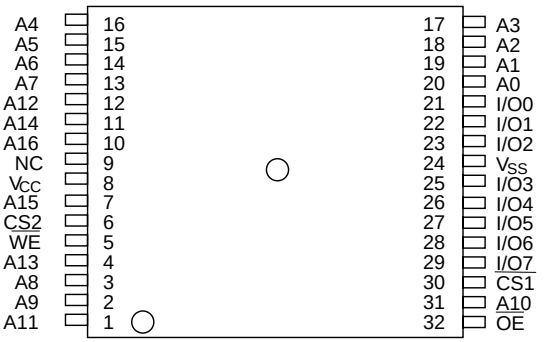
(Top View)

HM628128BT Series (Normal Type TSOP)



(Top View)

HM628128BR Series (Reverse Type TSOP)

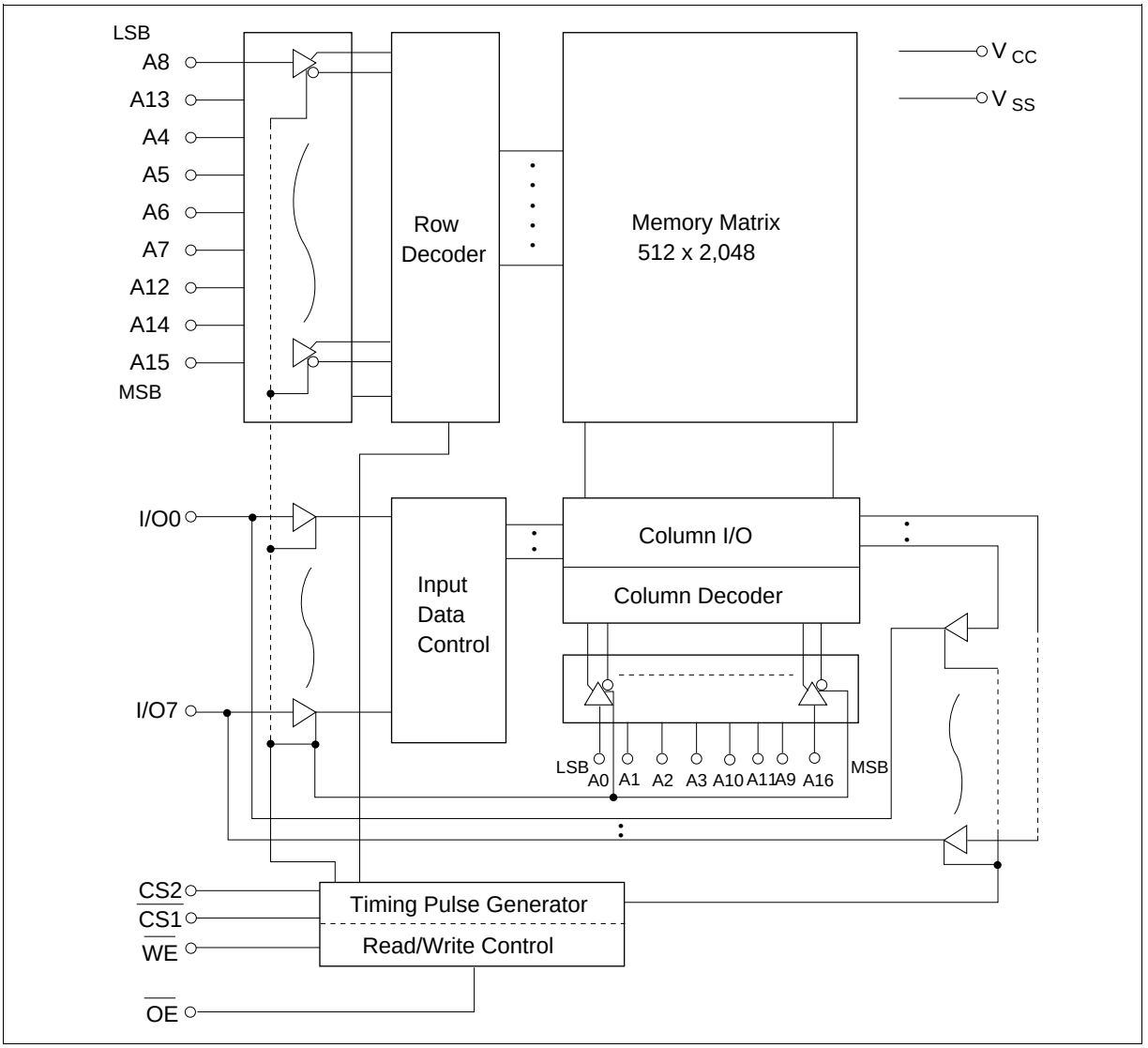


(Top View)

Pin Description

Pin Name	Function
A0 - A16	Address
I/O0 - I/O7	Input/output
$\overline{CS1}$	Chip select 1
CS2	Chip select 2
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
NC	No connection
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{CC}	–0.5 to +7.0	V
Voltage on any pin relative to V_{SS}	V_T	–0.5[*1] to V_{CC} + 0.3[*2]	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +85	°C

Notes: 1. –3.0 V for pulse half-width ≤ 30 ns
2. Maximum voltage is 7.0 V.

Function Table

$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
X	H	X	X	Not selected	I_{SB}, I_{SB1}	High-Z	—
X	X	L	X	Not selected	I_{SB}, I_{SB1}	High-Z	—
H	L	H	H	Output disable	I_{CC}	High-Z	—
H	L	H	L	Read	I_{CC}	Dout	Read cycle
L	L	H	H	Write	I_{CC}	Din	Write cycle (1)
L	L	H	L	Write	I_{CC}	Din	Write cycle (2)

Note: 1. X: H or L

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high voltage (logic 1)	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input low voltage (logic 0)	V_{IL}	–0.3[*1]	—	0.8	V

Note: 1. –3.0 V for pulse half-width ≤ 30ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10 %, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ[*1]	Max	Unit	Test conditions
Input leakage current	$\|I_{LI}\|$	—	—	1	µA	Vin = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	1	µA	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating power supply current : DC	I_{CC}	—	15	25	mA	$\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL}, $I_{I/O}$ = 0mA
Operating power supply current	I_{CC1}	—	35	70	mA	Min.cycle, duty = 100 %, $\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA
	I_{CC2}	—	10	20	mA	Cycle time = 1 µs, duty = 100 %, $I_{I/O}$ = 0 mA, $\overline{CS1}$ ≤ 0.2 V, CS2 ≥ V_{CC} – 0.2 V, Others = V_{IH}/V_{IL}, V_{IH} ≥ V_{CC} – 0.2 V, V_{IL} ≤ 0.2 V
Standby V_{CC} current : DC	I_{SB}	—	1	2	mA	CS2 = V_{IL} or CS2 = V_{IH}, $\overline{CS1}$ = V_{IH}
Standby V_{CC} current (1): DC	I_{SB1}	—	2[*2]	100[*2]	µA	0V≤ Vin ≤ V_{CC} , (1) 0 V≤ CS2 ≤ 0.2V or (2) CS2 ≥ V_{CC} – 0.2V , $\overline{CS1}$ ≥ V_{CC} – 0.2V
		—	2[*3]	50[*3]	µA	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –1.0 mA

Notes: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and not guaranteed.
2. For L-version
3. For L-SL version

Capacitance (Ta = 25°C, f = 1.0 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin[*1]	—	—	8	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$[*1]	—	—	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100 % tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ±10%, unless otherwise noted.)

Test Conditions

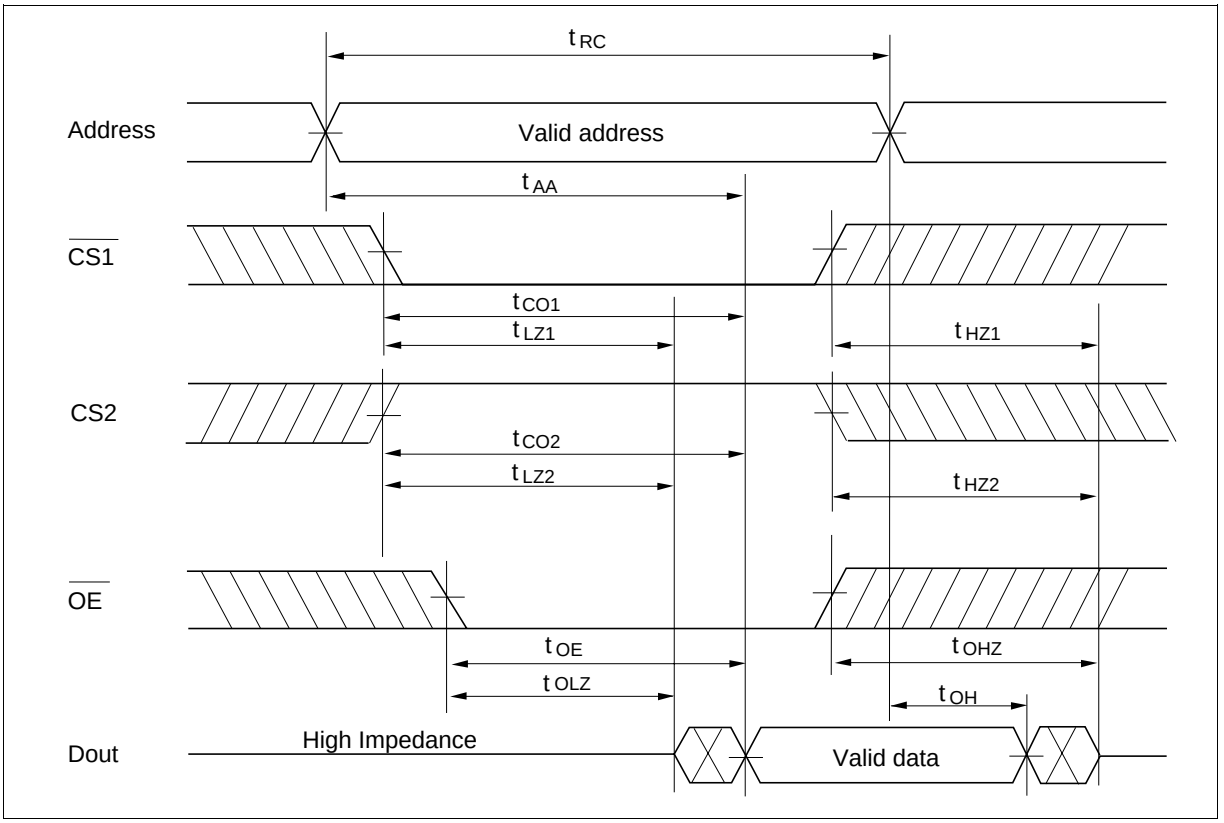
- Input pulse levels : 0.8 V to 2.4 V
- Input rise and fall time : 5 ns
- Input and output timing reference levels : 1.5 V
- Output load : 1 TTL Gate and C_L (100 pF) (Including scope and jig)

Read Cycle

		HM628128B					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read cycle time	t_{RC}	70	—	85	—	ns	
Address access time	t_{AA}	—	70	—	85	ns	
Chip selection to output valid	t_{CO1}	—	70	—	85	ns	
	t_{CO2}	—	70	—	85	ns	
Output enable to output valid	t_{OE}	—	35	—	45	ns	
Chip selection to output in low-Z	t_{LZ1}	10	—	10	—	ns	2, 3
	t_{LZ2}	10	—	10	—	ns	2, 3
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	ns	2, 3
Chip deselection to output in high-Z	t_{HZ1}	0	25	0	30	ns	1, 2, 3
	t_{HZ2}	0	25	0	30	ns	1, 2, 3
Output disable to output in high-Z	t_{OHZ}	0	25	0	30	ns	1, 2, 3
Output hold from address change	t_{OH}	10	—	10	—	ns	

Notes: 1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device to device.
3. This parameter is sampled and not 100% tested.

Read Cycle Timing ($\overline{WE}$ = V_{IH})

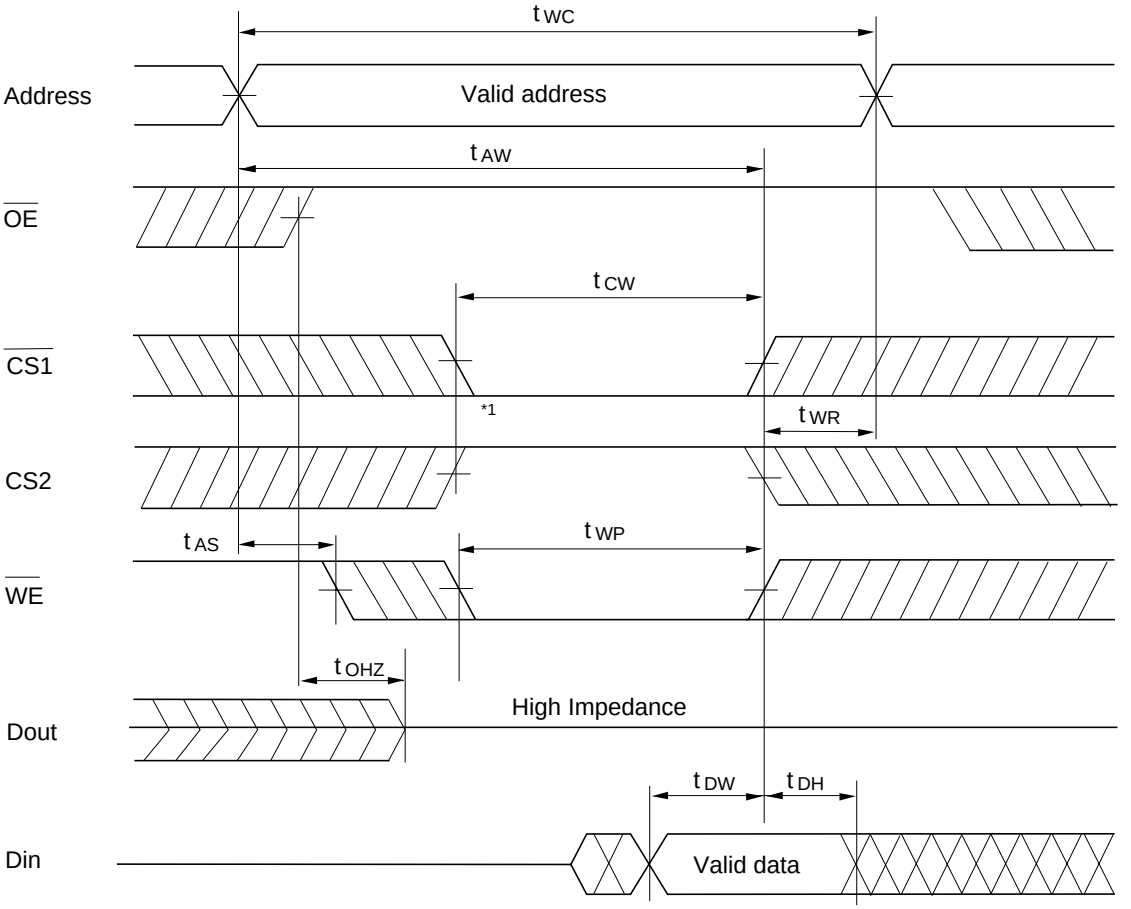


Write Cycle

		HM628128B					
		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write cycle time	t_{WC}	70	—	85	—	ns	
Chip selection to end of write	t_{CW}	60	—	75	—	ns	2
Address setup time	t_{AS}	0	—	0	—	ns	3
Address valid to end of write	t_{AW}	60	—	75	—	ns	
Write pulse width	t_{WP}	50	—	55	—	ns	1, 7
Write recovery time	t_{WR}	0	—	0	—	ns	4
Write to output in high-Z	t_{WHZ}	0	25	0	30	ns	5, 6
Data to write time overlap	t_{DW}	30	—	35	—	ns	
Write hold from write time	t_{DH}	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	ns	6
Output disable to output in High-Z	t_{OHZ}	0	25	0	25	ns	5

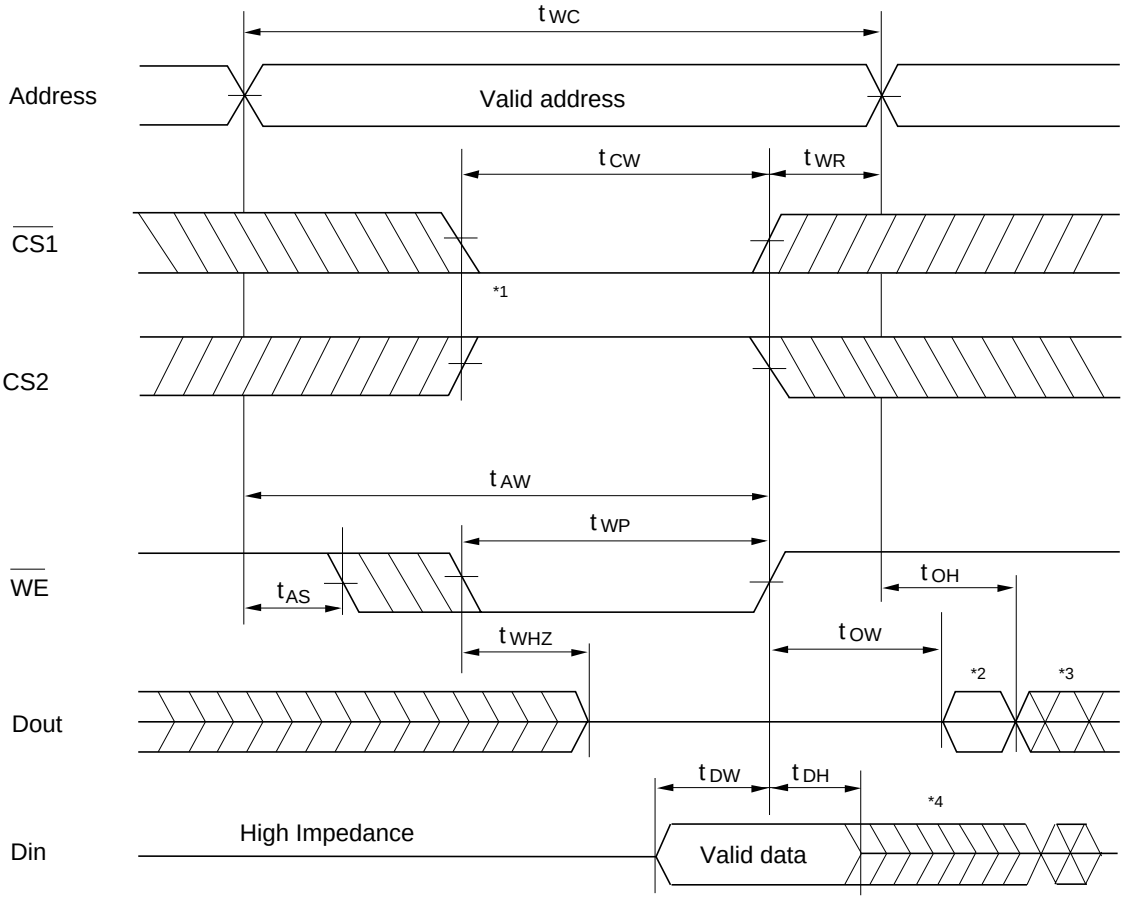
Notes:
1. A write occures during the overlap of a low $\overline{CS1}$, a high CS2, and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high, and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low, and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of write cycle.
5. During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.
6. This parameter is sampled and not 100% tested.
7. In the write cycle with $\overline{OE}$ low fixed, t_{WP} must satisfy the following equation to avoid a problem of date bus contention, $t_{WP} \geq t_{DW}$ (min) + t_{WHZ} (mix).

Write Cycle Timing (1) ($\overline{OE}$ Clock)



Note: 1. If the $\overline{CS1}$ goes low or CS2 goes high simultaneously with $\overline{WE}$ going low or after the $\overline{WE}$ going low, the outputs remain in a high impedance state.

Write Cycle Timing (2) ($\overline{OE}$ low fix)



Notes: 1. If the $\overline{CS1}$ goes low or CS2 goes high simultaneously with $\overline{WE}$ going low or after the $\overline{WE}$ going low, the outputs remain in a high impedance state.

2. Dout is the same phase of the latest written data in this write cycle.

3. Dout is the read date of next address.

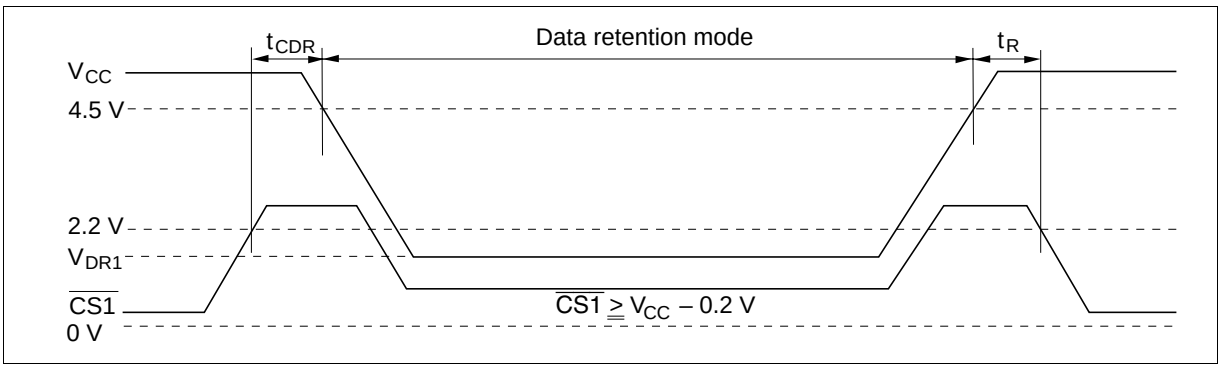
4. If $\overline{CS1}$ is low and CS2 high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

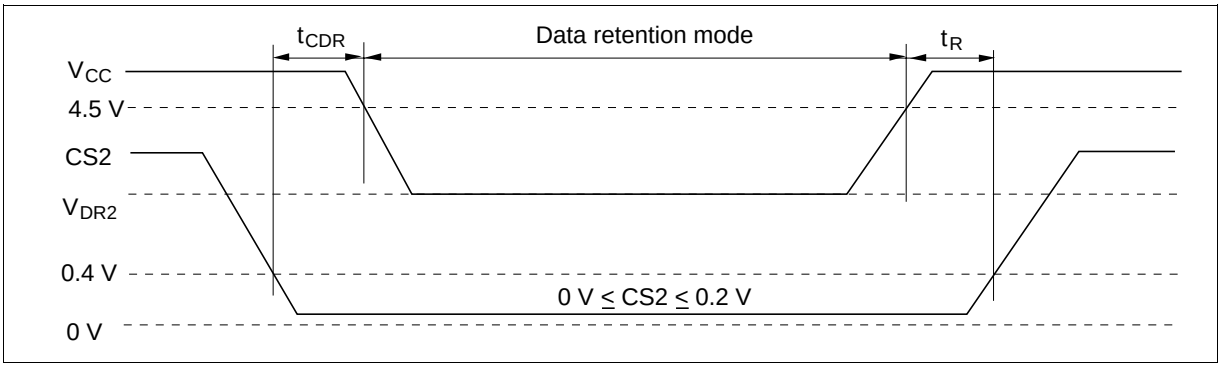
Parameter	Symbol		Min	Typ[*3]	Max	Unit	Test conditions[*4]
V_{CC} for data retention	V_{DR}		2.0	—	—	V	0 V ≤ Vin ≤ V_{CC}, (1) 0 V ≤ CS2 ≤ 0.2 V or (2) CS2 ≥ V_{CC} – 0.2 V, $\overline{CS1}$ ≥ V_{CC} – 0.2 V
Data retention current	I_{CCDR}	(L)	—	1	50[*1]	µA	V_{CC} = 3 V, 0 V ≤ Vin ≤ 3 V (1) 0 V ≤ CS2 ≤ 0.2 V or (2) CS2 ≥ V_{CC} – 0.2 V, $\overline{CS1}$ ≥ V_{CC} – 0.2 V
		(L-SL)	—	1	15[*2]	µA	
Chip deselect to data retention time	t_{CDR}		0	—	—	ns	See retention waveform
Operation recovery time	t_R		5	—	—	ms	

Notes: 1. This characteristics is guaranteed only for L-version, 20 µA max at Ta = 0 to 40°C.
2. This characteristics is guaranteed only for L-SL version, 3 µA max at Ta = 0 to 40°C.
3. Typical values are at V_{CC} = 3.0 V, Ta = +25°C and not guaranteed.
4. CS2 controls address buffer, $\overline{WE}$ buffer, $\overline{CS1}$ buffer, $\overline{OE}$ buffer, and Din buffer. If CS2 controls data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{CS1}$, I/O) can be in the high impedance state. If $\overline{CS1}$ controls data retention mode, CS2 must be CS2 ≥ V_{SS} – 0.2 V or 0 V ≤ CS2 ≤ 0.2 V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

Low V_{CC} Data Retention Waveform (1) ($\overline{CS1}$ Controlled)

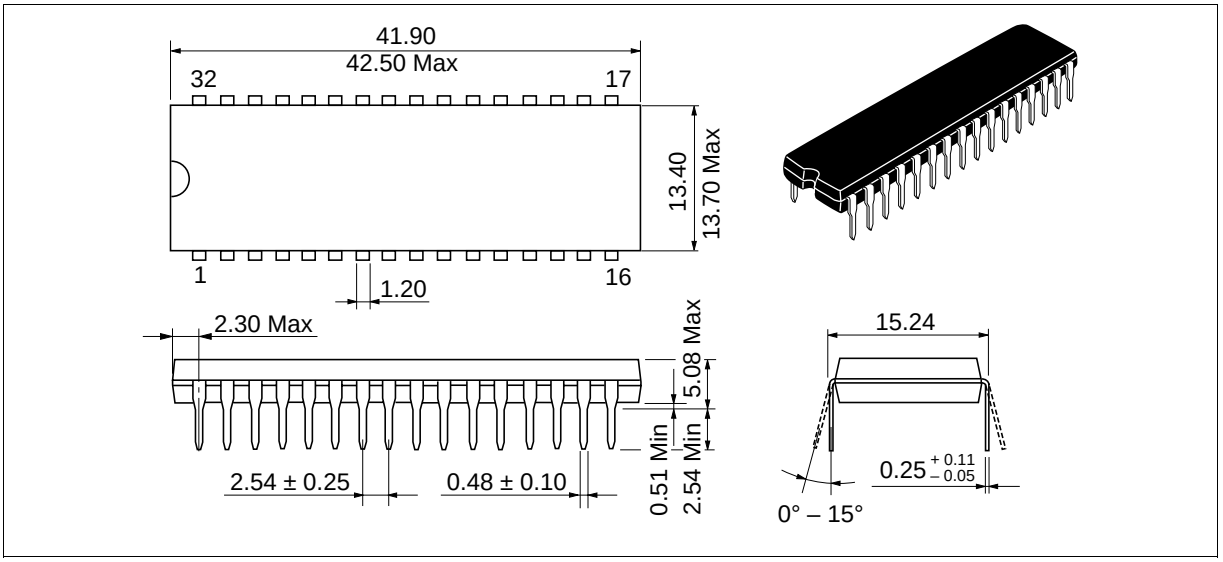


Low V_{CC} Data Retention Waveform (2) (CS2 Controlled)

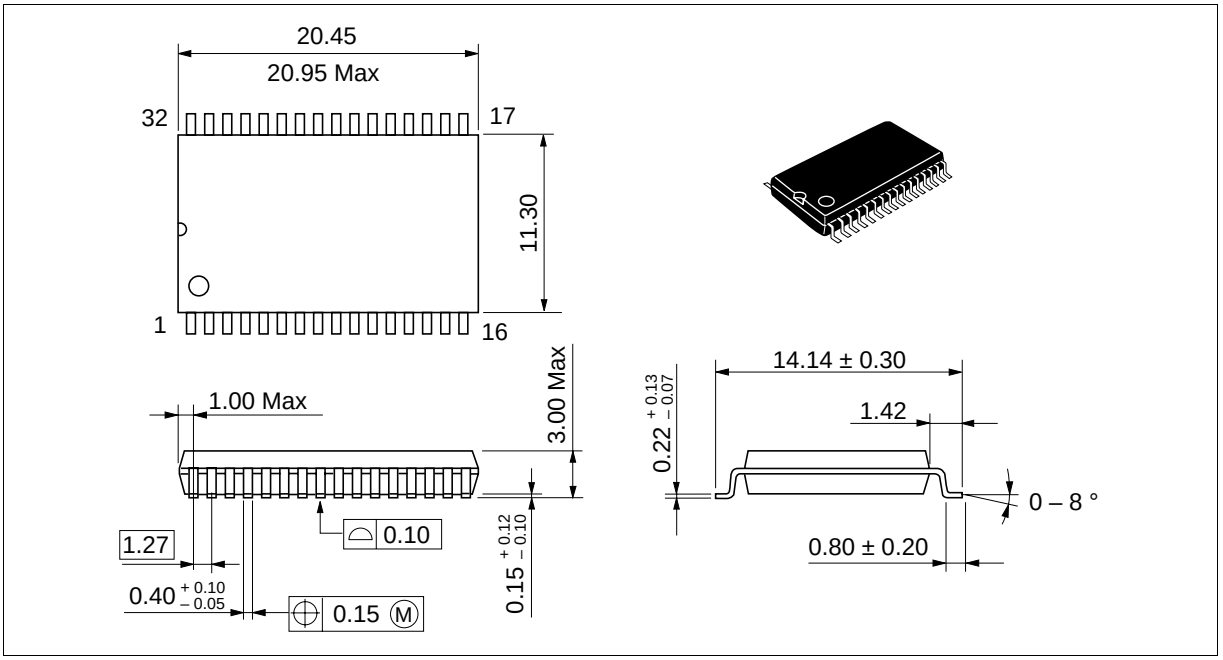


Package Dimensions

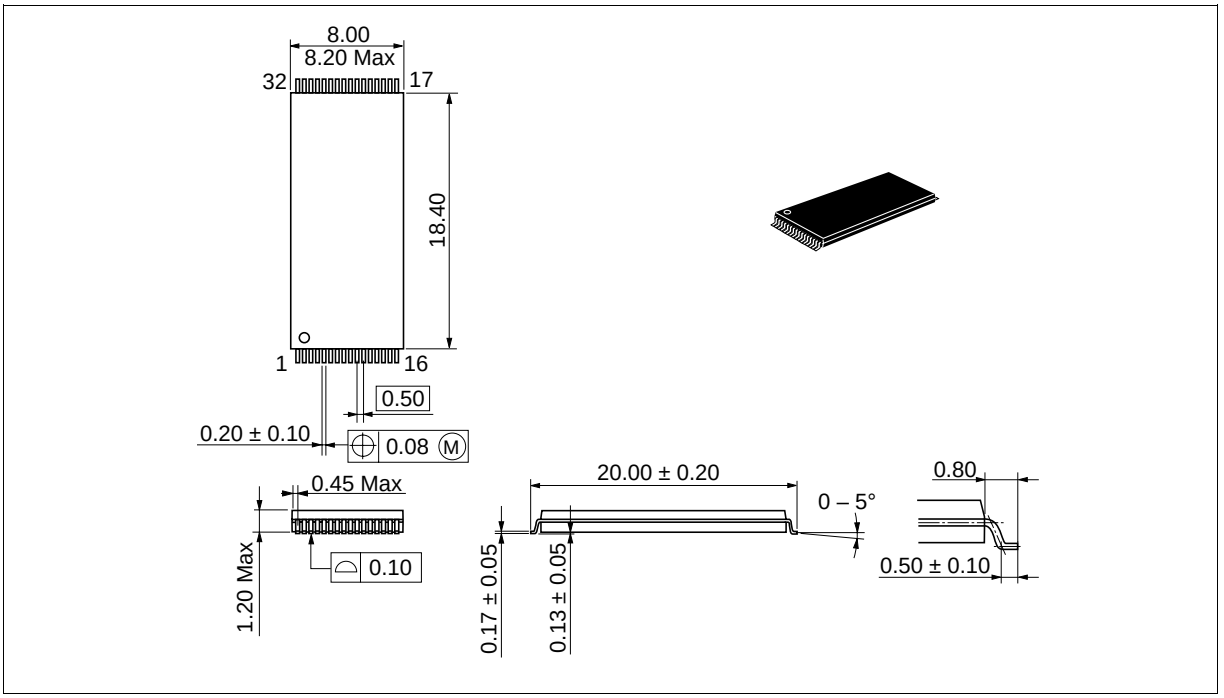
HM628128BLP Series (DP-32) Unit: mm



HM628128BLFP Series (FP-32D) Unit: mm



HM628128BLT Series (TFP-32D) Unit: mm



HM628128BLR Series (TFP-32DR) Unit: mm