National Semiconductor™

Discrete POWER & Signal Technologies

Surface Mount Transistors

NPN Saturated Switches

Device No. (SOT-23 Mark)	Case Style	V_{CBO} (V) Min	V_{CEO} (V) Min	V_{EBO} (V) Min	I_{CBO} (nA) @ Max	V_{CB} (V)	h_{FE} Min	h_{FE} Max	@ I_C (mA)	& V_{CE} (V)	$V_{CE(SAT)}$ (V) Max	& $V_{BE(SAT)}$ (V) Max	@ I_C (mA) ($I_B = \frac{I_C}{10}$)	C_{ob} (pF) Max	f_T (MHz) Min	@ I_C (mA)	$t_{(off)}$ (ns) Max	Test Conditions	Process No.
MMBT2369 (1J)	TO-236 (49)	40	15	4.5	400	20	20		100	2	0.25	0.85	10	4	500	10	18	(Note 1)	21
							40	120	10	1									
MMBT2369A (1S)	**TO-236 (49)**	**40**	**15**	**4.5**	**400**	**20**	**20**		**100**	**1**	**0.2**	**0.85**	**10**	**4**	**500**	**10**	**18**	**(Note 1)**	**21 (5-24)**
							30		**30**	**0.4**	**0.2**	**1.15**	**30**						
							40	**120**	**10**	**1**									
							40		**10**	**0.35**	**0.5**	**1.6**	**100**						
MMPQ2369	**SO-16 (S3)**	**40**	**15**	**4.5**	**400**	**20**	**20**		**100**	**1**	**0.2**	**0.85**	**10**	**4**	**500**	**10**			**21 (5-24)**
							30		**30**	**0.4**	**0.2**	**1.15**	**30**						
							40	**120**	**10**	**1**									
							40		**10**	**0.35**	**0.5**	**1.6**	**100**						
MMPQ3725	**SO-16 (S3)**	**60**	**40**	**6**	**1700**	**60**	**25**		**1A**	**5**	**0.25**	**0.76**	**10**	**10**	**300**	**50**			**25 (5-59)**
							20		**800**	**2**	**0.26**	**0.86**	**100**						
							35		**500**	**1**	**0.4**	**1.1**	**300**						
							40		**300**	**1**	**0.25**	**1.2**	**500**						
							60	**150**	**100**	**1**	**0.8**	**1.5**	**800**						
							30		**10**	**1**	**0.95**	**1.7**	**1A**						

TEST CONDITIONS

Note 1: V_{CC} = 3V, I_C = 10 mA, $I_B{}^1$ = 3 mA, $I_R{}^2$ = 1.5 mA.

Note 2: V_{CC} = 10V, I_C = 300 mA, $I_B{}^1$ = $I_B{}^2$ = 30 mA.

Note 3: V_{CC} = 30V, I_C = 500 mA, $I_B{}^1$ = $I_B{}^2$ = 50 mA.

NOTE: National preferred device for each process in **bold**. Number shown in parentheses indicates location **(section-page)** of device datasheet.