TEXAS INSTRUMENTS

LF198-N, LF298, LF398-N
LF198A-N, LF398A-N

SNOSBI3C – JULY 2000 – REVISED OCTOBER 2018

LFx98x Monolithic Sample-and-Hold Circuits

1 Features

- Operates from ±5-V to ±18-V Supplies
- Less than 10-μs Acquisition Time
- Logic Input Compatible With TTL, PMOS, CMOS
- 0.5-mV Typical Hold Step at Ch = 0.01 μF
- Low Input Offset
- 0.002% Gain Accuracy
- Low Output Noise in Hold Mode
- Input Characteristics Do Not Change During Hold Mode
- High Supply Rejection Ratio in Sample or Hold
- Wide Bandwidth
- Space Qualified, JM38510

2 Applications

- Ramp Generators With Variable Reset Level
- Integrators With Programmable Reset Level
- Synchronous Correlators
- 2-Channel Switches
- DC and AC Zeroing
- Staircase Generators

3 Description

The LFx98x devices are monolithic sample-and-hold circuits that use BI-FET technology to obtain ultrahigh DC accuracy with fast acquisition of signal and low droop rate. Operating as a unity-gain follower, DC gain accuracy is 0.002% typical and acquisition time is as low as 6 μs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin and does not degrade input offset drift. The wide bandwidth allows the LFx98x to be included inside the feedback loop of 1-MHz operational amplifiers without having stability problems. Input impedance of 10^{10} Ω allows high-source impedances to be used without degrading accuracy.

P-channel junction FETs are combined with bipolar devices in the output amplifier to give droop rates as low as 5 mV/min with a 1-μF hold capacitor. The JFETs have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design ensures no feedthrough from input to output in the hold mode, even for input signals equal to the supply voltages.

Logic inputs on the LFx98x are fully differential with low input current, allowing for direct connection to TTL, PMOS, and CMOS. Differential threshold is 1.4 V. The LFx98x will operate from ±5-V to ±18-V supplies.

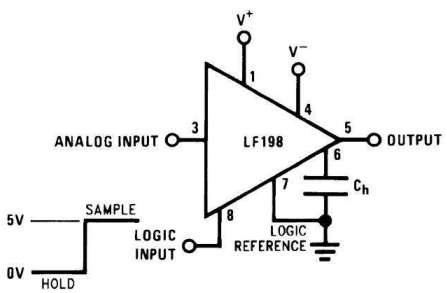
An A version is available with tightened electrical specifications.

Device Information(1)

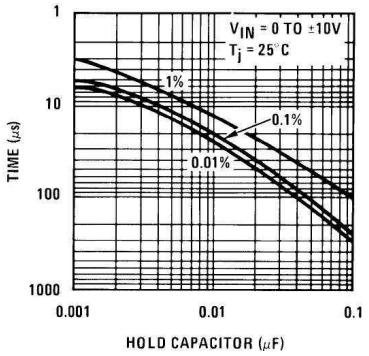
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LF298, LF398-N	SOIC (14)	8.65 mm × 3.91 mm
LFx98x	TO-99 (8)	9.08 mm × 9.08 mm
LF398-N	PDIP (8)	9.81 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Connection



Acquisition Time



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4 Revision History

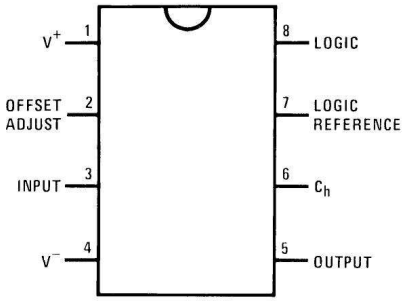
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (October 2015) to Revision C	Page
• Updated *Device Information* and *Pin Functions* tables	1
• Separated *Electrical Characteristics* into four tables: LF198-N and LF298; LF198A-N; LF398-N; and LF398A-N (OBSOLETE)	5

Changes from Revision A (July 2000) to Revision B	Page
• Added *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

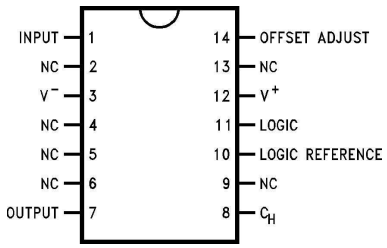
5 Pin Configuration and Functions

P Package
8-Pin PDIP
Top View

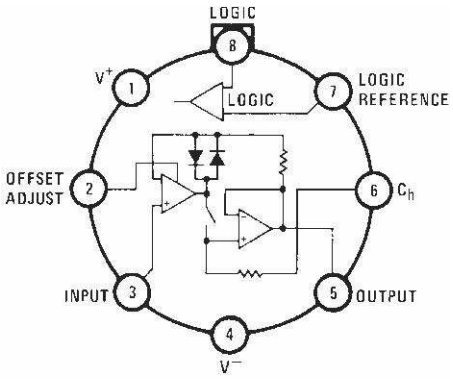


TOP VIEW

D Package
14-Pin SOIC
Top View



LMC Package
8-Pin TO-99
Top View



TOP VIEW

A military RETS electrical test specification is available on request. The LF198-N may also be procured to Standard Military Drawing #5962-8760801GA or to MIL-STD-38510 part ID JM38510/12501SGA.

Pin Functions

PIN				TYPE(1)	DESCRIPTION
NAME	LF298, LF398-N	LFx98x	LF398-N		
	SOIC-14	TO-99	PDIP-8		
V^+	12	1	1	P	Positive supply
OFFSET ADJUST	14	2	2	A	DC offset compensation pin
INPUT	1	3	3	A	Analog Input
V^-	3	4	4	P	Negative supply
OUTPUT	7	5	5	O	Output
C_h	8	6	6	A	Hold capacitor
LOGIC REFERENCE	10	7	7	I	Reference for LOGIC input
LOGIC	11	8	8	I	Logic input for Sample and Hold modes
NC	2, 4, 5, 6, 9, 13	—	—	NA	No connect

(1) P = Power, G = Ground, I = Input, O = Output, A = Analog

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Supply voltage			±18	V
Power dissipation	(Package limitation, see (3))		500	mW
Operating ambient temperature	LF198-N, LF198A-N	–55	125	°C
	LF298	–25	85	°C
	LF398-N, LF398A-N	0	70	°C
Input voltage			±18	V
Logic-to-logic reference differential voltage (see (4))		7	−30	V
Output short circuit duration		Indefinite		
Hold capacitor short circuit duration			10	sec
Lead temperature	H package (soldering, 10 sec.)		260	°C
	N package (soldering, 10 sec.)		260	°C
	M package: vapor phase (60 sec.)		215	°C
	Infrared (15 sec.)		220	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A) / R_{\theta JA}$, or the number given in the Absolute Maximum Ratings, whichever is lower. The maximum junction temperature, T_{JMAX}, for the LF198-N and LF198A-N is 150°C; for the LF298, 115°C; and for the LF398-N and LF398A-N, 100°C.
(4) Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2 V below the positive supply and 3 V above the negative supply.

6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Supply voltage			±15		V
T_J	Ambient temperature	LF198-N, LF198A-N	–55		125	°C
		LF298	–25		85	
		LF398-N, LF398A-N	0		70	

6.3 Thermal Information

THERMAL METRIC(1)		LF398-N	LF298, LF398-N	LFx98x	UNIT
		P (PDIP)	D (SOIC)	LMC (TO-99)	
		8 PINS	14 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	48.9	80.6	85(2)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.3	38.1	20	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	26.2	35.4	—	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.3	5.8	—	°C/W
ψ_{JB}	Junction-to-board characterization parameter	26.0	35.1	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Board mount in 400 LF/min air flow.

6.4 Electrical Characteristics, LF198-N and LF298

The following specifications apply for $-V_S + 3.5\ V \le V_{IN} \le +V_S - 3.5\ V$, $+V_S = +15\ V$, $-V_S = -15\ V$, $T_A = T_J = 25°C$, $C_h = 0.01\ \mu F$, $R_L = 10\ k\Omega$, LOGIC REFERENCE = 0 V, LOGIC HIGH = 2.5 V, LOGIC LOW = 0 V unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input offset voltage(1)	$T_J = 25°C$		1	3	mV
	Full temperature range			5	mV
Input bias current(1)	$T_J = 25°C$		5	25	nA
	Full temperature range			75	nA
Input impedance	$T_J = 25°C$		10		GΩ
Gain error	$T_J = 25°C$, $R_L = 10\ k$		0.002%	0.005%	
	Full temperature range			0.02%	
Feedthrough attenuation ratio at 1 kHz	$T_J = 25°C$, $C_h = 0.01\ \mu F$	86	96		dB
Output impedance	$T_J = 25°C$, "HOLD" mode		0.5	2	Ω
	Full temperature range			4	Ω
HOLD step(2)	$T_J = 25°C$, $C_h = 0.01\ \mu F$, $V_{OUT} = 0$		0.5	2	mV
Supply current(1)	$T_J \ge 25°C$		4.5	5.5	mA
Logic and logic reference input current	$T_J = 25°C$		2	10	μA
Leakage current into hold capacitor(1)	$T_J = 25°C$, hold mode(3)		30	100	pA
Acquisition time to 0.1%	$\Delta V_{OUT} = 10\ V$, $C_h = 1000\ pF$		4		μs
	$C_H = 0.01\ \mu F$		20		μs
Hold capacitor charging current	$V_{IN} - V_{OUT} = 2\ V$		5		mA
Supply voltage rejection ratio	$V_{OUT} = 0$	80	110		dB
Differential logic threshold	$T_J = 25°C$	0.8	1.4	2.4	V

(1) These parameters ensured over a supply voltage range of ±5 to ±18 V, and an input range of $-V_S + 3.5\ V \le V_{IN} \le +V_S - 3.5\ V$.
(2) Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1 pF, for instance, will create an additional 0.5-mV step with a 5-V logic swing and a 0.01-μF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.
(3) Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.

6.5 Electrical Characteristics, LF198A-N

The following specifications apply for $-V_S + 3.5\ V \le V_{IN} \le +V_S - 3.5\ V$, $+V_S = +15\ V$, $-V_S = -15\ V$, $T_A = T_J = 25°C$, $C_h = 0.01\ \mu F$, $R_L = 10\ k\Omega$, LOGIC REFERENCE = 0 V, LOGIC HIGH = 2.5 V, LOGIC LOW = 0 V unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input offset voltage(1)	$T_J = 25°C$		1	1	mV
	Full temperature range			2	mV
Input bias current(1)	$T_J = 25°C$		5	25	nA
	Full temperature range			75	nA
Input impedance	$T_J = 25°C$		10		GΩ
Gain error	$T_J = 25°C$, $R_L = 10\ k$		0.002%	0.005%	
	Full temperature range			0.01%	
Feedthrough attenuation ratio at 1 kHz	$T_J = 25°C$, $C_h = 0.01\ \mu F$	86	96		dB
Output impedance	$T_J = 25°C$, "HOLD" mode		0.5	1	Ω
	Full temperature range			4	Ω
HOLD step(2)	$T_J = 25°C$, $C_h = 0.01\ \mu F$, $V_{OUT} = 0$		0.5	1	mV
Supply current(1)	$T_J \ge 25°C$		4.5	5.5	mA
Logic and logic reference input current	$T_J = 25°C$		2	10	μA
Leakage current into hold capacitor(1)	$T_J = 25°C$, hold mode(3)		30	100	pA
Acquisition time to 0.1%	$\Delta V_{OUT} = 10\ V$, $C_h = 1000\ pF$		4	6	μs
	$C_H = 0.01\ \mu F$		20	25	μs
Hold capacitor charging current	$V_{IN} - V_{OUT} = 2\ V$		5		mA
Supply voltage rejection ratio	$V_{OUT} = 0$	90	110		dB
Differential logic threshold	$T_J = 25°C$	0.8	1.4	2.4	V

(1) These parameters ensured over a supply voltage range of ±5 to ±18 V, and an input range of $-V_S + 3.5\ V \le V_{IN} \le +V_S - 3.5\ V$.
(2) Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1 pF, for instance, will create an additional 0.5-mV step with a 5-V logic swing and a 0.01-μF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.
(3) Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.

6.6 Electrical Characteristics, LF398-N

The following specifications apply for $-V_S + 3.5\ V \le V_{IN} \le +V_S - 3.5\ V$, $+V_S = +15\ V$, $-V_S = -15\ V$, $T_A = T_J = 25°C$, $C_h = 0.01\ \mu F$, $R_L = 10\ k\Omega$, LOGIC REFERENCE = 0 V, LOGIC HIGH = 2.5 V, LOGIC LOW = 0 V unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input offset voltage(1)	$T_J = 25°C$		2	7	mV
	Full temperature range			10	mV
Input bias current(1)	$T_J = 25°C$		10	50	nA
	Full temperature range			100	nA
Input impedance	$T_J = 25°C$		10		GΩ
Gain error	$T_J = 25°C$, $R_L = 10\ k$		0.004%	0.01%	
	Full temperature range			0.02%	
Feedthrough attenuation ratio at 1 kHz	$T_J = 25°C$, $C_h = 0.01\ \mu F$	80	90		dB
Output impedance	$T_J = 25°C$, "HOLD" mode		0.5	4	Ω
	Full temperature range			6	Ω
HOLD step(2)	$T_J = 25°C$, $C_h = 0.01\ \mu F$, $V_{OUT} = 0$		1	2.5	mV
Supply current(1)	$T_J \ge 25°C$		4.5	6.5	mA
Logic and logic reference input current	$T_J = 25°C$		2	10	μA
Leakage current into hold capacitor(1)	$T_J = 25°C$, hold mode(3)		30	200	pA
Acquisition time to 0.1%	$\Delta V_{OUT} = 10\ V$, $C_h = 1000\ pF$		4		μs
	$C_H = 0.01\ \mu F$		20		μs
Hold capacitor charging current	$V_{IN} - V_{OUT} = 2\ V$		5		mA
Supply voltage rejection ratio	$V_{OUT} = 0$	80	110		dB
Differential logic threshold	$T_J = 25°C$	0.8	1.4	2.4	V

(1) These parameters ensured over a supply voltage range of ±5 to ±18 V, and an input range of $-V_S + 3.5\ V \le V_{IN} \le +V_S - 3.5\ V$.
(2) Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1 pF, for instance, will create an additional 0.5-mV step with a 5-V logic swing and a 0.01-μF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.
(3) Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.

6.7 Electrical Characteristics, LF398A-N (OBSOLETE)

The following specifications apply for $-V_S + 3.5\ V \le V_{IN} \le +V_S - 3.5\ V$, $+V_S = +15\ V$, $-V_S = -15\ V$, $T_A = T_J = 25°C$, $C_h = 0.01\ \mu F$, $R_L = 10\ k\Omega$, LOGIC REFERENCE = 0 V, LOGIC HIGH = 2.5 V, LOGIC LOW = 0 V unless otherwise specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input offset voltage(1)	$T_J = 25°C$		2	2	mV
	Full temperature range			3	mV
Input bias current(1)	$T_J = 25°C$		10	25	nA
	Full temperature range			50	nA
Input impedance	$T_J = 25°C$		10		GΩ
Gain error	$T_J = 25°C$, $R_L = 10\ k$		0.004%	0.005%	
	Full temperature range			0.01%	
Feedthrough attenuation ratio at 1 kHz	$T_J = 25°C$, $C_h = 0.01\ \mu F$	86	90		dB
Output impedance	$T_J = 25°C$, "HOLD" mode		0.5	1	Ω
	Full temperature range			6	Ω
HOLD step(2)	$T_J = 25°C$, $C_h = 0.01\ \mu F$, $V_{OUT} = 0$		1	1	mV
Supply current(1)	$T_J \ge 25°C$		4.5	6.5	mA
Logic and logic reference input current	$T_J = 25°C$		2	10	μA
Leakage current into hold capacitor(1)	$T_J = 25°C$, hold mode(3)		30	100	pA
Acquisition time to 0.1%	$\Delta V_{OUT} = 10\ V$, $C_h = 1000\ pF$		4	6	μs
	$C_H = 0.01\ \mu F$		20	25	μs
Hold capacitor charging current	$V_{IN} - V_{OUT} = 2\ V$		5		mA
Supply voltage rejection ratio	$V_{OUT} = 0$	90	110		dB
Differential logic threshold	$T_J = 25°C$	0.8	1.4	2.4	V

(1) These parameters ensured over a supply voltage range of ±5 to ±18 V, and an input range of $-V_S + 3.5\ V \le V_{IN} \le +V_S - 3.5\ V$.
(2) Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1 pF, for instance, will create an additional 0.5-mV step with a 5-V logic swing and a 0.01-μF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.
(3) Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.