



FEATURES

- Supports GR-1244 Stratum 3 stability in holdover mode
- Supports smooth reference switchover with virtually no disturbance on output phase
- Supports Telcordia GR-253 jitter generation, transfer, and tolerance for SONET/SDH up to OC-192 systems
- Supports ITU-T G.8262 synchronous Ethernet slave clocks
- Supports ITU-T G.823, G.824, G.825, and G.8261
- Auto/manual holdover and reference switchover
- 4 reference inputs (single-ended or differential)
- Input reference frequencies: 2 kHz to 1250 MHz
- Reference validation and frequency monitoring (1 ppm)
- Programmable input reference switchover priority
- 20-bit programmable input reference divider
- 6 pairs of clock output pins with each pair configurable as a single differential LVDS/HSTL output or as 2 single-ended CMOS outputs
- Output frequencies: 352 Hz to 1250 MHz
- Programmable 17-bit integer and 24-bit fractional feedback divider in digital PLL
- Programmable digital loop filter covering loop bandwidths from 0.1 Hz to 5 kHz (2 kHz maximum for <0.1 dB of peaking)
- Low noise system clock multiplier
- Frame sync support
- Adaptive clocking
- Optional crystal resonator for system clock input
- On-chip EEPROM to store multiple power-up profiles

Pin program function for easy frequency translation configuration

Software controlled power-down

64-lead, 9 mm × 9 mm, LFCSP package

APPLICATIONS

Network synchronization, including synchronous Ethernet and SDH to OTN mapping/demapping

Cleanup of reference clock jitter

SONET/SDH clocks up to OC-192, including FEC

Stratum 3 holdover, jitter cleanup, and phase transient control

Wireless base station controllers

Cable infrastructure

Data communications

GENERAL DESCRIPTION

The AD9558 is a low loop bandwidth clock multiplier that provides jitter cleanup and synchronization for many systems, including synchronous optical networks (SONET/SDH). The AD9558 generates an output clock synchronized to up to four external input references. The digital PLL allows for reduction of input time jitter or phase noise associated with the external references. The digitally controlled loop and holdover circuitry of the AD9558 continuously generates a low jitter output clock even when all reference inputs have failed.

The AD9558 operates over an industrial temperature range of -40°C to +85°C. If a smaller package is required, refer to the AD9557 for the two-input/two-output version of the same part.

FUNCTIONAL BLOCK DIAGRAM

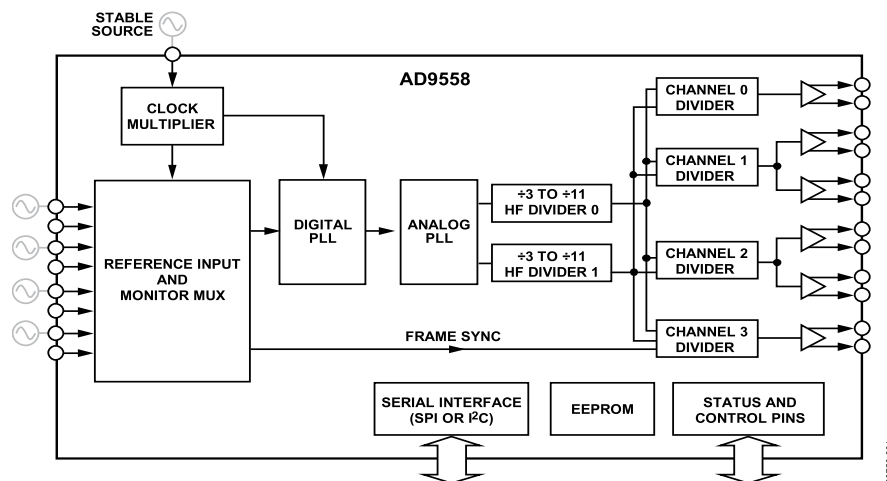


Figure 1.

Rev. A

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REVISION HISTORY

4/12—Rev 0 to Rev. A

Changed 3 Hz to 352 kHz in Output Frequencies List Item, Features Section	1
Change to Output Frequency Range Parameter, Min; and System Clock Input Doubler Duty Cycle Parameter Description, Table 6	6
Changes to Test Conditions/Comments Column, Table 9	8
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Changes to Pin 4 and Pin 42, Table 20	17
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Changed APLL VCO Lower Frequency and OUT5 Frequency Range, Figure 35; Changed 225 MHz to 200 MHz and 3.45 GHz to 3.35 GHz in Overview Section	29
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Changes to Figure 40; Changed 1024 to 1023 in Clock Dividers Section; Changes to Clock Distribution Synchronization Section	38
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10/11—Revision 0: Initial Version

SPECIFICATIONS

Minimum (min) and maximum (max) values apply for the full range of supply voltage and operating temperature variations. Typical (typ) values apply for AVDD3 = DVDD_I/O = 3.3 V; AVDD = DVDD = 1.8 V; T_A = 25°C, unless otherwise noted.

SUPPLY VOLTAGE

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY VOLTAGE					
DVDD3	3.135	3.30	3.465	V	
DVDD	1.71	1.80	1.89	V	
AVDD3	3.135	3.30	3.465	V	
AVDD	1.71	1.80	1.89	V	

SUPPLY CURRENT

The test conditions for the maximum (max) supply current are the same as the test conditions for the All Blocks Running parameter of Table 3. The test conditions for the typical (typ) supply current are the same as the test conditions for the Typical Configuration parameter of Table 3.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT FOR TYPICAL CONFIGURATION					Typical numbers are for the typical configuration listed in Table 3
I _{DVDD3}	12	19	26	mA	Pin 45, Pin 46, Pin 51, Pin 52, Pin 64
I _{DVDD}	12	20	28	mA	Pin 6, Pin 55, Pin 56
I _{AVDD3}	50	70	92	mA	Pin 25, Pin 26, Pin 31
I _{AVDD}	152	230	305	mA	Pin 7, Pin 10, Pin 12, Pin 17, Pin 22, Pin 29, Pin 30, Pin 35, Pin 37, Pin 38
SUPPLY CURRENT FOR THE ALL BLOCKS RUNNING CONFIGURATION					Maximum numbers are for all blocks running configuration in Table 3
I _{DVDD3}	23	34	46	mA	Pin 45, Pin 46, Pin 51, Pin 52, Pin 64
I _{DVDD}	11	22	32	mA	Pin 6, Pin 55, Pin 56
I _{AVDD3}	73	108	143	mA	Pin 25, Pin 26, Pin 31
I _{AVDD}	168	250	331	mA	Pin 7, Pin 10, Pin 12, Pin 17, Pin 22, Pin 29, Pin 30, Pin 35, Pin 37, Pin 38

POWER DISSIPATION

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER DISSIPATION					
Typical Configuration	0.47	0.74	1.02	W	System clock: 49.152 MHz crystal; DPLL active; both 19.44 MHz input references in differential mode; one HSTL driver at 644.53125 MHz; one 3.3 V CMOS driver at 161.1328125 MHz and 80 pF capacitive load on CMOS output
All Blocks Running	0.6	1.0	1.32	W	System clock: 49.152 MHz crystal; DPLL active; both input references in differential mode; four HSTL drivers at 750 MHz; four 3.3 V CMOS drivers at 250 MHz and 80 pF capacitive load on CMOS outputs
Full Power-Down		44	125	mW	Typical configuration with no external pull-up or pull-down resistors; about 2/3 of this power is on AVDD3
Incremental Power Dissipation					Conditions = typical configuration; table values show the change in power due to the indicated operation
Input Reference On/Off					
Differential Without Divide-by-2	20	25	32	mW	Additional current draw is in the DVDD3 domain only
Differential With Divide-by-2	26	32	40	mW	Additional current draw is in the DVDD3 domain only
Single-Ended (Without Divide-by-2)	5	7	9	mW	Additional current draw is in the DVDD3 domain only
Output Distribution Driver On/Off					
LVDS (at 750 MHz)	12	17	22	mW	Additional current draw is in the AVDD domain only
HSTL (at 750 MHz)	14	21	28	mW	Additional current draw is in the AVDD domain only
1.8 V CMOS (at 250 MHz)	14	21	28	mW	A single 1.8 V CMOS output with an 80 pF load
3.3 V CMOS (at 250 MHz)	18	27	36	mW	A single 3.3 V CMOS output with an 80 pF load
Other Blocks On/Off					
Second RF Divider	36	51	64	mW	Additional current draw is in the AVDD domain only
Channel Divider Bypassed	10	17	23	mW	Additional current draw is in the AVDD domain only

LOGIC INPUTS ($\overline{\text{SYNC}}$, $\overline{\text{RESET}}$, PINCONTROL, M7 TO M0)

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS ($\overline{\text{SYNC}}$, $\overline{\text{RESET}}$, PINCONTROL)					
Input High Voltage (V_{IH})	2.1			V	
Input Low Voltage (V_{IL})			0.8	V	
Input Current (I_{INH} , I_{INL})		± 50	± 100	μA	
Input Capacitance (C_{IN})		3		pF	
LOGIC INPUTS (M7 to M0)					
Input High Voltage (V_{IH})	2.5			V	
Input $\frac{1}{2}$ Level Voltage (V_{IM})	1.0		2.2	V	
Input Low Voltage (V_{IL})			0.6	V	
Input Current (I_{INH} , I_{INL})		± 60	± 100	μA	
Input Capacitance (C_{IN})		3		pF	

LOGIC OUTPUTS (M7 TO M0, IRQ)

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC OUTPUTS (M7 to M0, IRQ)					
Output High Voltage (V_{OH})	DVDD3 – 0.4			V	$I_{OH} = 1\text{ mA}$
Output Low Voltage (V_{OL})			0.4	V	$I_{OL} = 1\text{ mA}$
IRQ Leakage Current					Open-drain mode
Active Low Output Mode			–200	μA	$V_{OH} = 3.3\text{ V}$
Active High Output Mode			100	μA	$V_{OL} = 0\text{ V}$

SYSTEM CLOCK INPUTS (XOA, XOB)

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SYSTEM CLOCK MULTIPLIER					
Output Frequency Range	750		805	MHz	The VCO range may place limitations on nonstandard system clock input frequencies
Phase Frequency Detector (PFD) Rate			150	MHz	
Frequency Multiplication Range	2		255		Assumes valid system clock and PFD rates
SYSTEM CLOCK REFERENCE INPUT PATH					
Input Frequency Range	10		600	MHz	
Minimum Input Slew Rate	20			V/ μs	Minimum limit imposed for jitter performance
Common-Mode Voltage	1.05	1.16	1.25	V	Internally generated
Differential Input Voltage Sensitivity	250			mV p-p	Minimum voltage across pins required to ensure switching between logic states; the instantaneous voltage on either pin must not exceed the supply rails; can accommodate single-ended input by ac grounding of complementary input; 1 V p-p recommended for optimal jitter performance
System Clock Input Doubler Duty Cycle					This is the amount of duty cycle variation that can be tolerated on the system clock input to use the doubler
System Clock Input = 50 MHz	45	50	55	%	
System Clock Input = 20 MHz	46	50	54	%	
System Clock Input = 16 MHz to 20 MHz	47	50	53	%	
Input Capacitance		3		pF	Single-ended, each pin
Input Resistance		4.2		k Ω	
CRYSTAL RESONATOR PATH					
Crystal Resonator Frequency Range	10		50	MHz	Fundamental mode, AT cut crystal
Maximum Crystal Motional Resistance			100	Ω	

REFERENCE INPUTS

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIFFERENTIAL OPERATION					
Frequency Range					
Sinusoidal Input	10		750	MHz	
LVPECL Input	0.002		1250	MHz	The reference input divide-by-2 block must be engaged for $f_{IN} > 705$ MHz
LVDS Input	0.002		750	MHz	The reference input divide-by-2 block must be engaged for $f_{IN} > 705$ MHz
Minimum Input Slew Rate	40			V/ μ s	Minimum limit imposed for jitter performance
Common-Mode Input Voltage					
AC-Coupled	1.9	2	2.2	V	Internally generated
DC-Coupled	1.0		2.4	V	
Differential Input Voltage Sensitivity				mV	Minimum differential voltage across pins is required to ensure switching between logic levels; instantaneous voltage on either pin must not exceed the supply rails
$f_{IN} < 800$ MHz	240			mV	
$f_{IN} = 800$ to 1050 MHz	320			mV	
$f_{IN} = 1050$ to 1250 MHz	400			mV	
Differential Input Voltage Hysteresis		58	100	mV	
Input Resistance		21		k Ω	
Input Capacitance		3		pF	
Minimum Pulse Width High					
LVPECL	390			ps	
LVDS	640			ps	
Minimum Pulse Width Low					
LVPECL	390			ps	
LVDS	640			ps	
SINGLE-ENDED OPERATION					
Frequency Range (CMOS)	0.002		300	MHz	
Minimum Input Slew Rate	40			V/ μ s	Minimum limit imposed for jitter performance
Input Voltage High (V_{IH})					
1.2 V to 1.5 V Threshold Setting	1.0			V	
1.8 V to 2.5 V Threshold Setting	1.4			V	
3.0 V to 3.3 V Threshold Setting	2.0			V	
Input Voltage Low (V_{IL})					
1.2 V to 1.5 V Threshold Setting			0.35	V	
1.8 V to 2.5 V Threshold Setting			0.5	V	
3.0 V to 3.3 V Threshold Setting			1.0	V	
Input Resistance		47		k Ω	
Input Capacitance		3		pF	
Minimum Pulse Width High	1.5			ns	
Minimum Pulse Width Low	1.5			ns	

REFERENCE MONITORS

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE MONITORS					
Reference Monitor					
Loss of Reference Detection Time			1.1	DPLL PFD period	Nominal phase detector period = R/f_{REF}^1
Frequency Out-of-Range Limits	<2		10^5	$\Delta f/f_{REF}$ (ppm)	Programmable (lower bound is subject to quality of the system clock (SYSCLK)); SYSCLK accuracy must be better than the lower bound
Validation Timer	0.001		65.535	sec	Programmable in 1 ms increments

¹ f_{REF} is the frequency of the active reference; R is the frequency division factor determined by the R-divider.

REFERENCE SWITCHOVER SPECIFICATIONS

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE SWITCHOVER SPECIFICATIONS					
Maximum Output Phase Perturbation (Phase Build-Out Switchover)					Assumes a jitter-free reference; satisfies Telcordia GR-1244-CORE requirements; select high PM base loop filter bit (Register 0x070E, Bit 0) is set to 1 for all active references
50 Hz DPLL Loop Bandwidth					Valid for automatic and manual reference switching
Peak		0	± 100	ps	
Steady State		0	± 100	ps	
2 kHz DPLL Loop Bandwidth					Valid for automatic and manual reference switching
Peak		0	± 250	ps	
Steady State		0	± 100	ps	
Time Required to Switch to a New Reference					
Phase Build-Out Switchover			1.1	DPLL PFD period	Calculated using the nominal phase detector period ($NPDP = R/f_{REF}$); the total time required is equal to the time plus the reference validation time and the time required to lock to the new reference

DISTRIBUTION CLOCK OUTPUTS

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HSTL MODE					
Output Frequency	0.000352		1250	MHz	OUT5 only; OUT0 to OUT4 minimum output frequency is 360 kHz
Rise/Fall Time (20% to 80%) ¹		140	250	ps	100 Ω termination across output pins
Duty Cycle					
Up to $f_{OUT} = 700$ MHz	45	48	52	%	
Up to $f_{OUT} = 750$ MHz	42	48	53	%	
Up to $f_{OUT} = 1250$ MHz		43		%	
Differential Output Voltage Swing	700	950	1200	mV	Magnitude of voltage across pins; output driver static
Common-Mode Output Voltage	700	870	960	mV	Output driver static
LVDS MODE					
Output Frequency	0.000352		1250	MHz	OUT5 only; OUT0 to OUT4 minimum output frequency is 360 kHz
Rise/Fall Time (20% to 80%) ¹		185	280	ps	100 Ω termination across the output pair
Duty Cycle					
Up to $f_{OUT} = 750$ MHz	44	48	53	%	
Up to $f_{OUT} = 800$ MHz	43	47	53	%	
Up to $f_{OUT} = 1250$ MHz		43		%	
Differential Output Voltage Swing					
Balanced, V_{OD}	247		454	mV	Voltage swing between output pins; output driver static
Unbalanced, ΔV_{OD}			50	mV	Absolute difference between voltage swing of normal pin and inverted pin; output driver static
Offset Voltage					
Common-Mode, V_{OS}	1.125	1.26	1.375	V	Output driver static
Common-Mode Difference, ΔV_{OS}			50	mV	Voltage difference between pins; output driver static
Short-Circuit Output Current		13	24	mA	Output driver static
CMOS MODE					
Output Frequency					OUT5 only; OUT0 to OUT4 minimum output frequency is 360 kHz
1.8 V Supply	0.000352		150	MHz	10 pF load
3.3 V Supply (OUT0 and OUT5)					
Strong Drive Strength Setting	0.000352		250	MHz	10 pF load
Weak Drive Strength Setting	0.000352		25	MHz	10 pF load
Rise/Fall Time (20% to 80%) ¹					
1.8 V Supply		1.5	3	ns	10 pF load
3.3 V Supply					
Strong Drive Strength Setting		0.4	0.6	ns	10 pF load
Weak Drive Strength Setting		8		ns	10 pF load
Duty Cycle					
1.8 V Mode		50		%	10 pF load
3.3 V Strong Mode		47		%	10 pF load
3.3 V Weak Mode		51		%	10 pF load
Output Voltage High (V_{OH})					Output driver static; strong drive strength
AVDD3 = 3.3 V, $I_{OH} = 10$ mA	AVDD3 – 0.3			V	
AVDD3 = 3.3 V, $I_{OH} = 1$ mA	AVDD3 – 0.1			V	
AVDD3 = 1.8 V, $I_{OH} = 1$ mA	AVDD – 0.2			V	
Output Voltage Low (V_{OL})					Output driver static; strong drive strength
AVDD3 = 3.3 V, $I_{OL} = 10$ mA			0.3	V	
AVDD3 = 3.3 V, $I_{OL} = 1$ mA			0.1	V	
AVDD3 = 1.8 V, $I_{OL} = 1$ mA			0.1	V	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT TIMING SKEW					10 pF load
Between OUT0 and OUT1		10	70	ps	HSTL mode on both drivers; rising edge only; any divide value
Between OUT0 and OUT3		105	222	ps	HSTL mode on both drivers; rising edge only; any divide value
Between OUT0 and OUT5		1.39	1.76	ns	HSTL mode on both drivers; rising edge only; any divide value
Between OUT1 and OUT2 (OUT1 and OUT2 Share the Same Divider)		1	12	ps	HSTL mode on both drivers; rising edge only; any divide value
Between OUT3 and OUT4 (OUT3 and OUT4 Share the Same Divider)		1	24	ps	HSTL mode on both drivers; rising edge only; any divide value
Across All OUT0 to OUT4 HSTL		105	235	ps	HSTL mode on all drivers; rising edge only; any divide value
Across All OUT0 to OUT4 LVDS		100	235	ps	LVDS mode on all drivers; rising edge only; any divide value
Additional Delay on One Driver by Changing Its Logic Type					
HSTL to LVDS	−5	+1	+5	ps	Positive value indicates that the LVDS edge is delayed relative to HSTL
HSTL to 1.8 V CMOS	−5	0	+5	ps	Positive value indicates that the CMOS edge is delayed relative to HSTL
HSTL to 3.3 V CMOS, Strong Mode					The CMOS edge is delayed relative to HSTL
OUT0 CMOS to OUT1 HSTL		3.53	3.59	ns	
OUT0 CMOS to OUT3 HSTL		3.55	3.65	ns	
OUT0 CMOS to OUT4 HSTL		3.56	3.68	ns	
OUT0 CMOS to OUT5 HSTL		4.84	5.1	ns	

¹ The listed values are for the slower edge (rise or fall).

TIME DURATION OF DIGITAL FUNCTIONS

Table 11.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TIME DURATION OF DIGITAL FUNCTIONS					
EEPROM-to-Register Download Time		13	20	ms	Using default EEPROM storage sequence (see Register 0x0E10 to Register 0x0E3F)
Register-to-EEPROM Upload Time		138	145	ms	Using default EEPROM storage sequence (see Register 0x0E10 to Register 0x0E3F)
Minimum Power-Down Exit Time		1		ms	Time from power-down exit to system clock lock detect

DIGITAL PLL

Table 12.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL PLL					
Phase-Frequency Detector (PFD) Input Frequency Range	2		100	kHz	
Loop Bandwidth	0.1		2000	Hz	Programmable design parameter
Phase Margin	30		89	Degrees	Programmable design parameter
Closed-Loop Peaking	<0.1			dB	Programmable design parameter ; part can be programmed for <0.1 dB peaking in accordance with Telcordia GR-253 jitter transfer
Reference Input (R) Division Factor	1		2 ²⁰		1, 2, ..., 1,048,576
Integer Feedback (N1) Division Factor	180		2 ¹⁷		180, 181, ..., 131,072
Fractional Feedback Divide Ratio	0		0.999		Maximum value: 16,777,215/16,777,216

DIGITAL PLL LOCK DETECTION

Table 13.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PHASE LOCK DETECTOR					
Threshold Programming Range	0.001		65.5	ns	
Threshold Resolution		1		ps	
FREQUENCY LOCK DETECTOR					
Threshold Programming Range	0.001		16,700	ns	Reference-to-feedback period difference
Threshold Resolution		1		ps	

HOLDOVER SPECIFICATIONS

Table 14.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HOLDOVER SPECIFICATIONS					
Initial Frequency Accuracy		<0.01		ppm	Excludes frequency drift of SYSCLK source; excludes frequency drift of input reference prior to entering holdover; compliant with GR-1244 Stratum 3

SERIAL PORT SPECIFICATIONS—SPI MODE

Table 15.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
$\overline{\text{CS}}$					
Input Logic 1 Voltage		2.0		V	
Input Logic 0 Voltage		0.8		V	
Input Logic 1 Current		60		μA	
Input Logic 0 Current		100		μA	
Input Capacitance		2		pF	
SCLK					Internal 30 k Ω pull-down resistor
Input Logic 1 Voltage		2.0		V	
Input Logic 0 Voltage		0.8		V	
Input Logic 1 Current		200		μA	
Input Logic 0 Current		1		μA	
Input Capacitance		2		pF	
SDIO					
As an Input					
Input Logic 1 Voltage		2.0		V	
Input Logic 0 Voltage		0.8		V	
Input Logic 1 Current		1		μA	
Input Logic 0 Current		1		μA	
Input Capacitance		2		pF	
As an Output					
Output Logic 1 Voltage	DVDD3 – 0.6			V	1 mA load current
Output Logic 0 Voltage			0.4	V	1 mA load current
SDO					
Output Logic 1 Voltage	DVDD3 – 0.6			V	1 mA load current
Output Logic 0 Voltage			0.4	V	1 mA load current
TIMING					
SCLK					
Clock Rate, $1/t_{\text{CLK}}$			40	MHz	
Pulse Width High, t_{HIGH}	10			ns	
Pulse Width Low, t_{LOW}	13			ns	
SDIO to SCLK Setup, t_{DS}	3			ns	
SCLK to SDIO Hold, t_{DH}	6			ns	
SCLK to Valid SDIO and SDO, t_{DV}			10	ns	
$\overline{\text{CS}}$ to SCLK Setup (t_{S})	10			ns	
$\overline{\text{CS}}$ to SCLK Hold (t_{c})	0			ns	
$\overline{\text{CS}}$ Minimum Pulse Width High	6			ns	

SERIAL PORT SPECIFICATIONS—I²C MODE

Table 16.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SDA, SCL (AS INPUT)					
Input Logic 1 Voltage	0.7 × DVDD3			V	For V _{IN} = 10% to 90% DVDD3
Input Logic 0 Voltage			0.3 × DVDD3	V	
Input Current	−10		+10	μA	
Hysteresis of Schmitt Trigger Inputs	0.015 × DVDD3				
Pulse Width of Spikes That Must Be Suppressed by the Input Filter, t _{SP}			50	ns	
SDA (AS OUTPUT)					
Output Logic 0 Voltage			0.4	V	I _O = 3 mA 10 pF ≤ C _b ≤ 400 pF
Output Fall Time from V _{IHmin} to V _{ILmax}	20 + 0.1 C _b ¹		250	ns	
TIMING					
SCL Clock Rate			400	kHz	After this period, the first clock pulse is generated
Bus-Free Time Between a Stop and Start Condition, t _{BUF}	1.3			μs	
Repeated Start Condition Setup Time, t _{SU; STA}	0.6			μs	
Repeated Hold Time Start Condition, t _{HD; STA}	0.6			μs	
Stop Condition Setup Time, t _{SU; STO}	0.6			μs	
Low Period of the SCL Clock, t _{LOW}	1.3			μs	
High Period of the SCL Clock, t _{HIGH}	0.6			μs	
SCL/SDA Rise Time, t _R	20 + 0.1 C _b ¹		300	ns	
SCL/SDA Fall Time, t _F	20 + 0.1 C _b ¹		300	ns	
Data Setup Time, t _{SU; DAT}	100			ns	
Data Hold Time, t _{HD; DAT}	100			ns	
Capacitive Load for Each Bus Line, C _b ¹			400	pF	

¹ C_b is the capacitance (pF) of a single bus line.

JITTER GENERATION

Jitter generation (random jitter) uses 49.152 MHz crystal for system clock input.

Table 17.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
JITTER GENERATION					System clock doubler enabled; high phase margin mode enabled; Register 0x0405 = 0x20; Register 0x0403 = 0x07; Register 0x0400 = 0x81; in cases where multiple driver types are listed, both driver types were tested at those conditions, and the one with higher jitter is quoted, although there is usually not a significant jitter difference between the driver types
f _{REF} = 19.44 MHz; f _{OUT} = 622.08 MHz; f _{LOOP} = 50 Hz					
HSTL Driver					
Bandwidth: 5 kHz to 20 MHz		304		fs rms	
Bandwidth: 12 kHz to 20 MHz		296		fs rms	
Bandwidth: 20 kHz to 80 MHz		300		fs rms	
Bandwidth: 50 kHz to 80 MHz		266		fs rms	
Bandwidth: 16 MHz to 320 MHz		185		fs rms	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
$f_{REF} = 19.44 \text{ MHz}$; $f_{OUT} = 644.53 \text{ MHz}$; $f_{LOOP} = 50 \text{ Hz}$ HSTL and/or LVDS Driver					
Bandwidth: 5 kHz to 20 MHz		334		fs rms	
Bandwidth: 12 kHz to 20 MHz		321		fs rms	
Bandwidth: 20 kHz to 80 MHz		319		fs rms	
Bandwidth: 50 kHz to 80 MHz		277		fs rms	
Bandwidth: 16 MHz to 320 MHz		185		fs rms	
$f_{REF} = 19.44 \text{ MHz}$; $f_{OUT} = 693.48 \text{ MHz}$; $f_{LOOP} = 50 \text{ Hz}$ HSTL Driver					
Bandwidth: 5 kHz to 20 MHz		298		fs rms	
Bandwidth: 12 kHz to 20 MHz		285		fs rms	
Bandwidth: 20 kHz to 80 MHz		286		fs rms	
Bandwidth: 50 kHz to 80 MHz		252		fs rms	
Bandwidth: 16 MHz to 320 MHz		183		fs rms	
$f_{REF} = 19.44 \text{ MHz}$; $f_{OUT} = 174.703 \text{ MHz}$; $f_{LOOP} = 1 \text{ kHz}$ HSTL Driver					
Bandwidth: 5 kHz to 20 MHz		354		fs rms	
Bandwidth: 12 kHz to 20 MHz		301		fs rms	
Bandwidth: 20 kHz to 80 MHz		321		fs rms	
Bandwidth: 50 kHz to 80 MHz		290		fs rms	
Bandwidth: 4 MHz to 80 MHz		177		fs rms	
$f_{REF} = 19.44 \text{ MHz}$; $f_{OUT} = 174.703 \text{ MHz}$; $f_{LOOP} = 100 \text{ Hz}$ LVDS and/or 3.3 V CMOS Driver					
Bandwidth: 5 kHz to 20 MHz		306		fs rms	
Bandwidth: 12 kHz to 20 MHz		293		fs rms	
Bandwidth: 20 kHz to 80 MHz		313		fs rms	
Bandwidth: 50 kHz to 80 MHz		283		fs rms	
Bandwidth: 4 MHz to 80 MHz		166		fs rms	
$f_{REF} = 25 \text{ MHz}$; $f_{OUT} = 161.1328 \text{ MHz}$; $f_{LOOP} = 100 \text{ Hz}$ HSTL Driver					
Bandwidth: 5 kHz to 20 MHz		316		fs rms	
Bandwidth: 12 kHz to 20 MHz		302		fs rms	
Bandwidth: 20 kHz to 80 MHz		324		fs rms	
Bandwidth: 50 kHz to 80 MHz		292		fs rms	
Bandwidth: 4 MHz to 80 MHz		171		fs rms	
$f_{REF} = 2 \text{ kHz}$; $f_{OUT} = 70.656 \text{ MHz}$; $f_{LOOP} = 100 \text{ Hz}$; HSTL and/or 3.3 V CMOS Driver					
Bandwidth: 10 Hz to 30 MHz		3.22		ps rms	
Bandwidth: 5 kHz to 20 MHz		338		fs rms	
Bandwidth: 12 kHz to 20 MHz		324		fs rms	
Bandwidth: 10 kHz to 400 kHz		278		fs rms	
Bandwidth: 100 kHz to 10 MHz		210		fs rms	
$f_{REF} = 25 \text{ MHz}$; $f_{OUT} = 1 \text{ GHz}$; $f_{LOOP} = 500 \text{ Hz}$ HSTL Driver					
Bandwidth: 100 Hz to 500 MHz (Broadband)		1.71		ps rms	
Bandwidth: 12 kHz to 20 MHz		343		fs rms	
Bandwidth: 20 kHz to 80 MHz		338		fs rms	

Jitter generation (random jitter) uses 19.2 MHz TCXO for system clock input.

Table 18.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
JITTER GENERATION					System clock doubler enabled; high phase margin mode enabled; Register 0x0405 = 0x20; Register 0x0403 = 0x07; Register 0x0400 = 0x81; in cases where multiple driver types are listed, both driver types were tested at those conditions, and the one with higher jitter is quoted, although there is usually not a significant jitter difference between the driver types
$f_{REF} = 19.44 \text{ MHz}$; $f_{OUT} = 644.53 \text{ MHz}$; $f_{LOOP} = 0.1 \text{ Hz}$ HSTL Driver					
Bandwidth: 5 kHz to 20 MHz		402		fs rms	
Bandwidth: 12 kHz to 20 MHz		393		fs rms	
Bandwidth: 20 kHz to 80 MHz		391		fs rms	
Bandwidth: 50 kHz to 80 MHz		347		fs rms	
Bandwidth: 16 MHz to 320 MHz		179		fs rms	
$f_{REF} = 19.44 \text{ MHz}$; $f_{OUT} = 693.48 \text{ MHz}$; $f_{LOOP} = 0.1 \text{ Hz}$ HSTL Driver					
Bandwidth: 5 kHz to 20 MHz		379		fs rms	
Bandwidth: 12 kHz to 20 MHz		371		fs rms	
Bandwidth: 20 kHz to 80 MHz		371		fs rms	
Bandwidth: 50 kHz to 80 MHz		335		fs rms	
Bandwidth: 16 MHz to 320 MHz		175		fs rms	
$f_{REF} = 19.44 \text{ MHz}$; $f_{OUT} = 312.5 \text{ MHz}$; $f_{LOOP} = 0.1 \text{ Hz}$ HSTL Driver					
Bandwidth: 5 kHz to 20 MHz		413		fs rms	
Bandwidth: 12 kHz to 20 MHz		404		fs rms	
Bandwidth: 20 kHz to 80 MHz		407		fs rms	
Bandwidth: 50 kHz to 80 MHz		358		fs rms	
Bandwidth: 4 MHz to 80 MHz		142		fs rms	
$f_{REF} = 25 \text{ MHz}$; $f_{OUT} = 161.1328 \text{ MHz}$; $f_{LOOP} = 0.1 \text{ Hz}$ HSTL Driver					
Bandwidth: 5 kHz to 20 MHz		399		fs rms	
Bandwidth: 12 kHz to 20 MHz		391		fs rms	
Bandwidth: 20 kHz to 80 MHz		414		fs rms	
Bandwidth: 50 kHz to 80 MHz		376		fs rms	
Bandwidth: 4 MHz to 80 MHz		190		fs rms	
$f_{REF} = 2 \text{ kHz}$; $f_{OUT} = 70.656 \text{ MHz}$; $f_{LOOP} = 0.1 \text{ Hz}$ HSTL and/or 3.3 V CMOS Driver					
Bandwidth: 10 Hz to 30 MHz		970		fs rms	
Bandwidth: 12 kHz to 20 MHz		404		fs rms	
Bandwidth: 10 kHz to 400 kHz		374		fs rms	
Bandwidth: 100 kHz to 10 MHz		281		fs rms	

ABSOLUTE MAXIMUM RATINGS

Table 19.

Parameter	Rating
Analog Supply Voltage (AVDD)	2 V
Digital Supply Voltage (DVDD)	2 V
Digital I/O Supply Voltage (DVDD3)	3.6 V
Analog Supply Voltage (AVDD3)	3.6 V
Maximum Digital Input Voltage	−0.5 V to DVDD3 + 0.5 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.