Dual 8A per Channel Low V_{IN} DC/DC µModule Regulator

FEATURES

- **Complete Dual DC/DC Regulator System**
- **Input Voltage Range: 2.7V to 5.5V**
- **Dual 8A Outputs, or Single 16A Output with a 0.6V to 5V Range**
- **Output Voltage Tracking and Margining**
- **±1.75% Total DC Output Error (–55°C to 125°C)**
- **Current Mode Control/Fast Transient Response**
- **Power Good Tracking and Margining**
- **Overcurrent/Thermal Shutdown Protection**
- **Onboard Frequency Synchronization**
- **Spread Spectrum Frequency Modulation**
- **Multiphase Operation**
- Selectable Burst Mode® Operation
- Output Overvoltage Protection
- SnPb (BGA) or RoHS Compliant (LGA and BGA) Finish
- Small Surface Mount Footprint, Low Profile (15mm × 15mm × 2.82mm) LGA and (15mm × 15mm × 3.42mm) BGA Packages

APPLICATIONS

- Telecom, Networking and Industrial Equipment
- Storage and ATCA, PCI Express Cards
- Battery Operated Equipment

DESCRIPTION

The LTM®4616 is a complete dual 2-phase 8A per channel switch mode DC/DC power regulator system in a 15mm × 15mm surface mount LGA or BGA package. Included in the package are the switching controller, power FETs, inductor and all support components. Operating from an input voltage range of 2.7V to 5.5V, the LTM4616 supports two outputs within a voltage range of 0.6V to 5V, each set by a single external resistor. This high efficiency design delivers up to 8A continuous current (10A peak) for each output. Only bulk input and output capacitors are needed, depending on ripple requirement. The part can also be configured for a 2-phase single output at up to 16A.

The low profile package enables utilization of unused space on the back side of PC boards for high density point-of-load regulation.

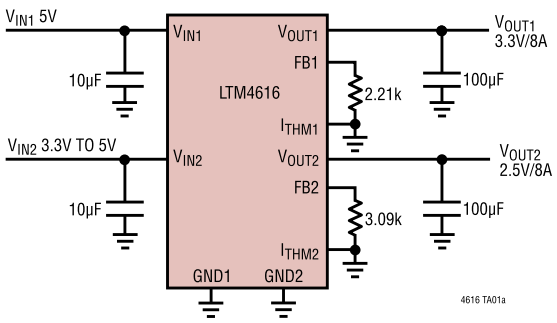
Fault protection features include overvoltage protection, overcurrent protection and thermal shutdown. The power module is offered in space saving and thermally enhanced 15mm × 15mm × 2.82mm LGA and 15mm × 15mm × 3.42mm BGA packages. The LTM4616 is available with SnPb (BGA) or RoHS compliant terminal finish.

Different Combinations of Input and Output

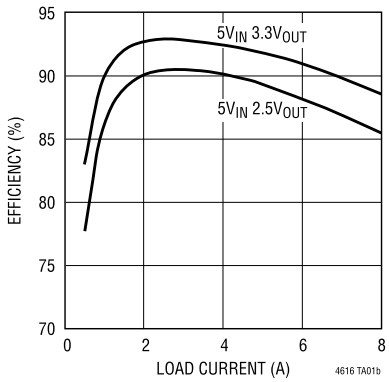
Number of Inputs	Number of Outputs	I_{OUT} (MAX)
2	2	8A, 8A
2	1	16A
1	2	8A, 8A
1	1	16A

TYPICAL APPLICATION

Dual Output DC/DC µModule® Regulator



Efficiency vs Load Current

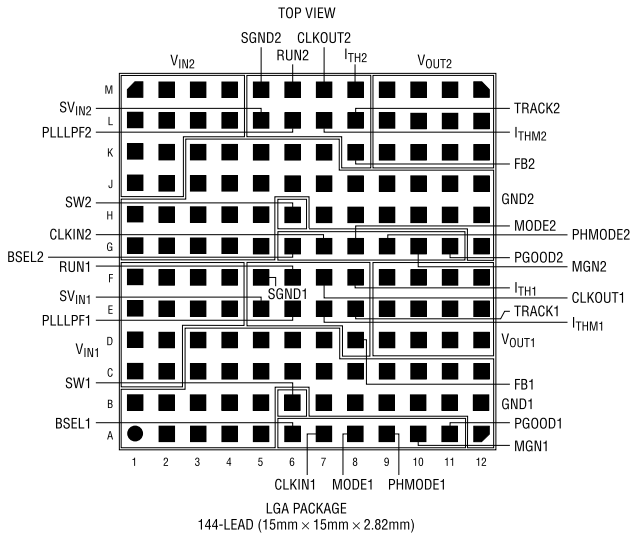


ABSOLUTE MAXIMUM RATINGS

(Note 1)

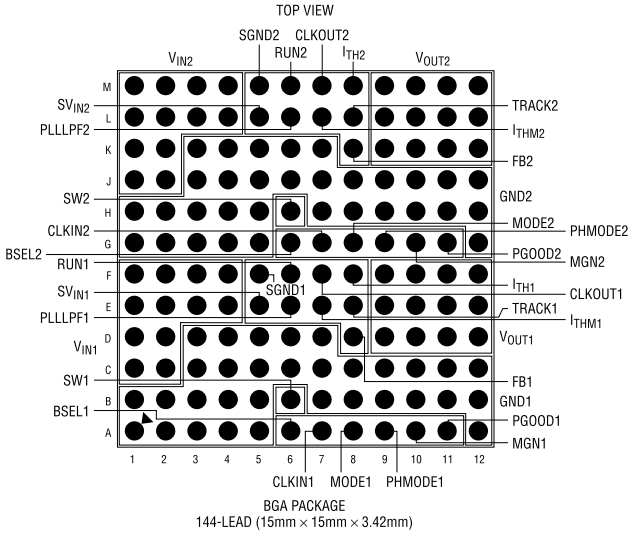
V_{IN1}, SV_{IN1}, V_{IN2}, SV_{IN2} ..... –0.3V to 6V
CLKOUT1, CLKOUT2 ..... –0.3V to 2V
PGOOD1, PLLLPF1, CLKIN1, PHMODE1, MODE1, PGOOD2, PLLLPF2, CLKIN2, PHMODE2, MODE2 ..... –0.3V to V_{IN}
I_{TH1}, I_{THM1}, RUN1, FB1, TRACK1, MGN1, BSEL1, I_{TH2}, I_{THM2}, RUN2, FB2, TRACK2, MGN2, BSEL2 ..... –0.3V to V_{IN}
V_{OUT1}, V_{OUT2}, SW1, SW2 ..... –0.3V to V_{IN}
Internal Operating Temperature Range (Note 2)
E- and I-Grades ..... –40°C to 125°C
MP-Grade ..... –55°C to 125°C
Junction Temperature ..... 125°C
Storage Temperature Range ..... –55°C to 125°C

PIN CONFIGURATION



LGA PACKAGE
144-LEAD (15mm × 15mm × 2.82mm)

T_{JMAX} = 125°C, θ_{JA} = 10.5°C/W, $\theta_{JCbottom}$ = 2°C/W, θ_{JCtop} = 16°C/W, WEIGHT = 1.8g
θ_{JA} DERIVED FROM 95mm × 76mm PCB WITH 4 LAYERS



BGA PACKAGE
144-LEAD (15mm × 15mm × 3.42mm)

T_{JMAX} = 125°C, θ_{JA} = 10.5°C/W, $\theta_{JCbottom}$ = 2°C/W, θ_{JCtop} = 16°C/W, WEIGHT = 2.0g
θ_{JA} DERIVED FROM 95mm × 76mm PCB WITH 4 LAYERS

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (Note 2)
		DEVICE	FINISH CODE			
LTM4616EV#PBF	Au (RoHS)	LTM4616V	e4	LGA	3	–40°C to 125°C
LTM4616IV#PBF	Au (RoHS)	LTM4616V	e4	LGA	3	–40°C to 125°C
LTM4616MPV#PBF	Au (RoHS)	LTM4616V	e4	LGA	3	–55°C to 125°C
LTM4616EY#PBF	SAC305 (RoHS)	LTM4616Y	e1	BGA	3	–40°C to 125°C
LTM4616IY#PBF	SAC305 (RoHS)	LTM4616Y	e1	BGA	3	–40°C to 125°C
LTM4616IY	SnPb (63/37)	LTM4616Y	e0	BGA	3	–40°C to 125°C
LTM4616MPY#PBF	SAC305 (RoHS)	LTM4616Y	e1	BGA	3	–55°C to 125°C
LTM4616MPY	SnPb (63/37)	LTM4616Y	e0	BGA	3	–55°C to 125°C

Consult Marketing for parts specified with wider operating temperature ranges. *Device temperature grade is indicated by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.

- Pb-free and Non-Pb-free Part Markings: www.linear.com/leadfree
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures: www.linear.com/umodule/pcbassembly
- LGA and BGA Package and Tray Drawings: www.linear.com/packaging

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). T_A = 25°C, V_{IN} = 5V unless otherwise noted. Per the typical application in Figure 18. Specified as each channel (Note 3).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN1(DC)}$, $V_{IN2(DC)}$	Input DC Voltage		●	2.7		5.5	V
$V_{OUT1(DC)}$, $V_{OUT2(DC)}$	Output Voltage, Total Variation with Line and Load	C_{IN} = 10µF × 1, C_{OUT} = 100µF Ceramic, 100µF POSCAP, R_{FB} = 6.65k, MODE = 0V V_{IN} = 2.7V to 5.5V, I_{OUT} = $I_{OUT(DC)MIN}$ to $I_{OUT(DC)MAX}$ (Note 4)	 ●	 1.472 1.464	 1.49 1.49	 1.508 1.516	 V V
Input Specifications							
$V_{IN1(UVLO)}$, $V_{IN2(UVLO)}$	Undervoltage Lockout Threshold	SV_{IN} Rising SV_{IN} Falling		2.05 1.85	2.2 2.0	2.35 2.15	V V
$I_{Q(VIN1, VIN2)}$	Input Supply Bias Current	V_{IN} = 3.3V, V_{OUT} = 1.5V, No Switching, MODE = V_{IN} V_{IN} = 3.3V, V_{OUT} = 1.5V, No Switching, MODE = 0V V_{IN} = 3.3V, V_{OUT} = 1.5V, Switching Continuous			400 1.15 55		µA mA mA
		V_{IN} = 5V, V_{OUT} = 1.5V, No Switching, MODE = V_{IN} V_{IN} = 5V, V_{OUT} = 1.5V, No Switching, MODE = 0V V_{IN} = 5V, V_{OUT} = 1.5V, Switching Continuous			450 1.3 75		µA mA mA
		Shutdown, RUN = 0, V_{IN} = 5V			1		µA
$I_{S(VIN1, VIN2)}$	Input Supply Current	V_{IN} = 3.3V, V_{OUT} = 1.5V, I_{OUT} = 8A V_{IN} = 5V, V_{OUT} = 1.5V, I_{OUT} = 8A			4.5 2.93		A A
Output Specifications							
$I_{OUT1(DC)}$, $I_{OUT2(DC)}$	Output Continuous Current Range	V_{OUT} = 1.5V (Note 4) V_{IN} = 3.3V, 5.5V V_{IN} = 2.7V		 0 0		 8 5	 A A
$\Delta V_{OUT1(LINE)}/V_{OUT1}$ $\Delta V_{OUT2(LINE)}/V_{OUT2}$	Line Regulation Accuracy	V_{OUT} = 1.5V, V_{IN} from 2.7V to 5.5V, I_{OUT} = 0A	●		0.1	0.25	%/V
$\Delta V_{OUT1(LOAD)}/V_{OUT1}$ $\Delta V_{OUT2(LOAD)}/V_{OUT2}$	Load Regulation Accuracy	V_{OUT} = 1.5V (Note 4) V_{IN} = 3.3V, 5.5V, I_{LOAD} = 0A to 8A V_{IN} = 2.7V, I_{LOAD} = 0A to 5A	 ● ●		 0.3 0.3	 0.5 0.5	 % %
$V_{OUT1(AC)}$, $V_{OUT2(AC)}$	Output Ripple Voltage	I_{OUT} = 0A, C_{OUT} = 100µF X5R Ceramic, V_{IN} = 5V, V_{OUT} = 1.5V			10		mV_{P-P}
f_{S1}, f_{S2}	Switching Frequency	I_{OUT} = 8A, V_{IN} = 5V, V_{OUT} = 1.5V		1.25	1.5	1.75	MHz
f_{SYNC1}, f_{SYNC2}	SYNC Capture Range			0.75		2.25	MHz
$\Delta V_{OUT1(START)}$, $\Delta V_{OUT2(START)}$	Turn-On Overshoot	C_{OUT} = 100µF, V_{OUT} = 1.5V, I_{OUT} = 0A V_{IN} = 3.3V V_{IN} = 5V		 	 10 10	 	 mV mV
t_{START1}, t_{START2}	Turn-On Time	C_{OUT} = 100µF, V_{OUT} = 1.5V, V_{IN} = 5V, I_{OUT} = 1A Resistive Load, Track = V_{IN}			100		µs
$\Delta V_{OUT1(LS)}$, $\Delta V_{OUT2(LS)}$	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load, C_{OUT} = 100µF Ceramic x2, 470µF POSCAP, V_{IN} = 5V, V_{OUT} = 1.5V			20		mV
$t_{SETTLE1}$, $t_{SETTLE2}$	Settling Time for Dynamic Load Step	Load: 0% to 50% to 0% of Full Load, V_{IN} = 5V, V_{OUT} = 1.5V, C_{OUT} = 100µF			10		µs
$I_{OUT1(PK)}$, $I_{OUT2(PK)}$	Output Current Limit	C_{OUT} = 100µF V_{IN} = 2.7V, V_{OUT} = 1.5V V_{IN} = 3.3V, V_{OUT} = 1.5V V_{IN} = 5V, V_{OUT} = 1.5V			 8 11 13		 A A A

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). T_A = 25°C, V_{IN} = 5V unless otherwise noted. Per the typical application in Figure 18. Specified as each channel (Note 3).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Control Section							
FB1, FB2	Voltage at FB Pin	I_{OUT} = 0A, V_{OUT} = 1.5V, V_{IN} = 2.7V to 5.5V	 ●	0.590 0.587	0.596 0.596	0.602 0.606	V V
SS Delay	Internal Soft-Start Delay				90		µs
I_{FB1}, I_{FB2}					0.2		µA
V_{RUN1}, V_{RUN2}	RUN Pin On/Off Threshold	RUN Rising RUN Falling		1.4 1.3	1.55 1.4	1.7 1.5	V V
TRACK1, TRACK2	Tracking Threshold (Rising) Tracking Threshold (Falling) Tracking Disable Threshold	RUN = V_{IN} RUN = 0V			0.57 0.18 V_{IN} – 0.5		V V V
R_{FBHI1}, R_{FBHI2}	Resistor Between V_{OUT} and FB Pins			9.95	10	10.05	kΩ
ΔV_{PGOOD1}, ΔV_{PGOOD2}	PGOOD Range				±10		%
I_{PGOOD1}, I_{PGOOD2}	PGOOD Leakage Current	V_{PGOOD} = V_{IN} = 2.7V to 5.5V, I_{OUT} = $I_{OUT(DC)MAX}$ (Note 4)	●		20	30	µA
V_{PGL1}, V_{PGL2}	PGOOD Voltage Low	I_{PGOOD} = 5mA			0.2	0.4	V
%Margining	Output Voltage Margining Percentage	MGN = V_{IN}, BSEL = 0V MGN = V_{IN}, BSEL = V_{IN} MGN = V_{IN}, BSEL = Float MGN = 0V, BSEL = 0V MGN = 0V, BSEL = V_{IN} MGN = 0V, BSEL = Float		4 9 14 –4 –9 –14	5 10 15 –5 –10 –15	6 11 16 –6 –11 –16	% % % % % %

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

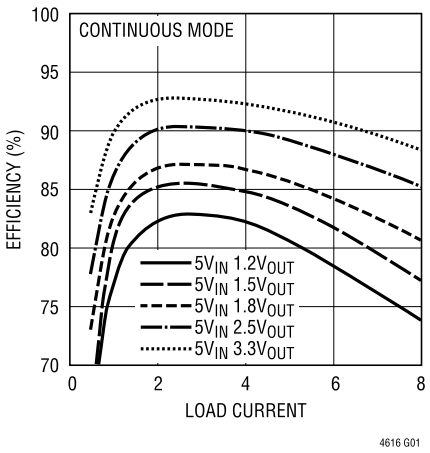
Note 2: The LTM4616 is tested under pulsed load conditions, such that $T_J \approx T_A$. The LTM4616E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4616I is guaranteed to meet specifications over the –40°C to 125°C internal operating temperature range. The LTM4616MP is guaranteed and tested over the –55°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: Two channels are tested separately and the same testing conditions are applied to each channel.

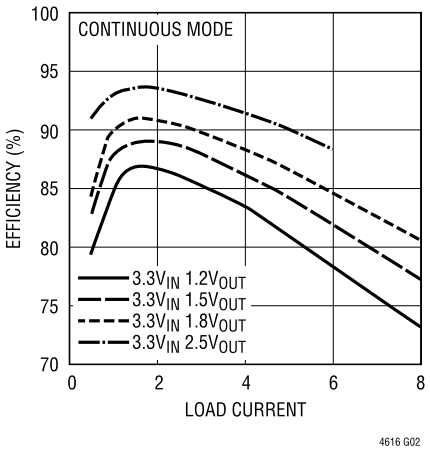
Note 4: See Output Current Derating curves for different V_{IN}, V_{OUT} and T_A.

TYPICAL PERFORMANCE CHARACTERISTICS Specified as Each Channel

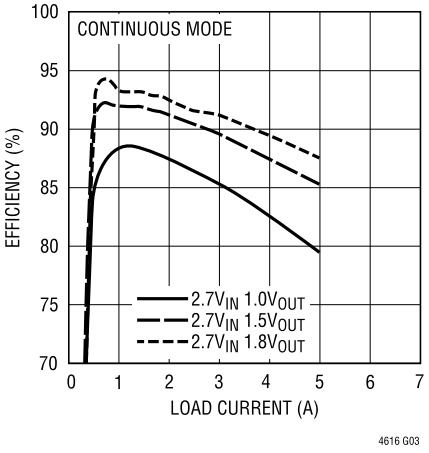
Efficiency vs Load Current



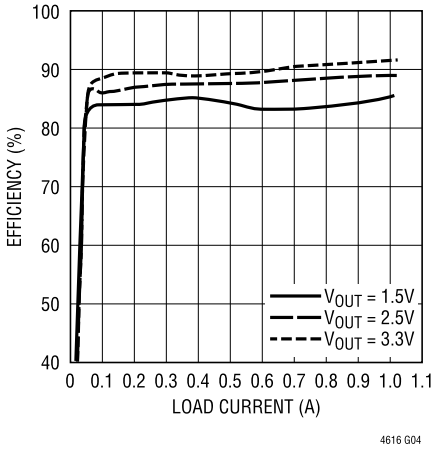
Efficiency vs Load Current



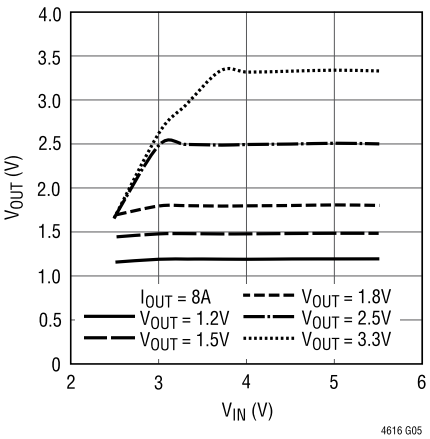
Efficiency vs Load Current



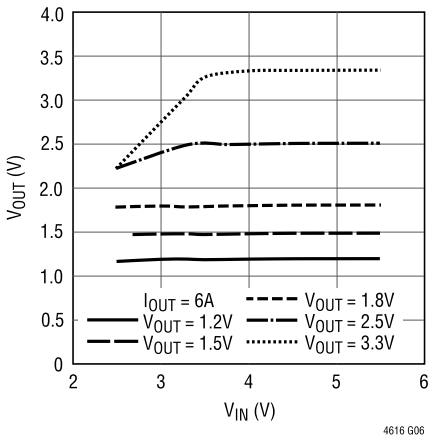
Burst Mode Efficiency with 5V Input



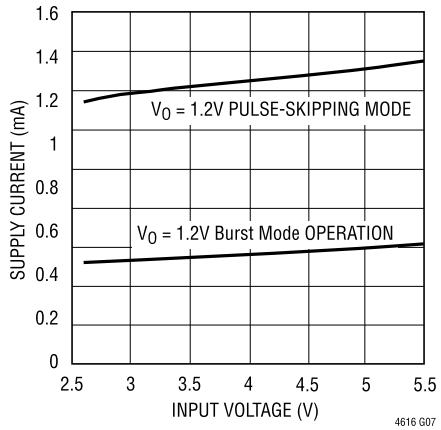
V_{IN} to V_{OUT} Step-Down Ratio



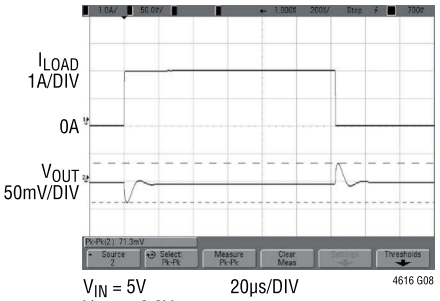
V_{IN} to V_{OUT} Step-Down Ratio



Supply Current vs V_{IN}

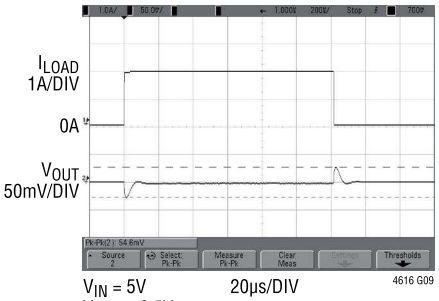


Load Transient Response



V_{IN} = 5V 20µs/DIV
V_{OUT} = 3.3V
2A/µs STEP
C_{OUT} = 2 × 100µF X5R, 470µF 4V POSCAP

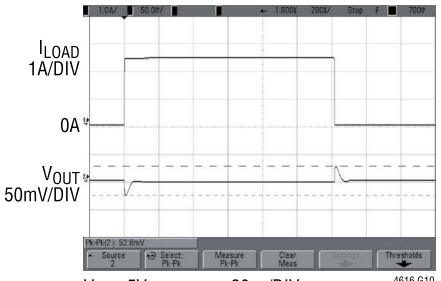
Load Transient Response



V_{IN} = 5V 20µs/DIV
V_{OUT} = 2.5V
2A/µs STEP
C_{OUT} = 2 × 100µF X5R, 470µF 4V POSCAP

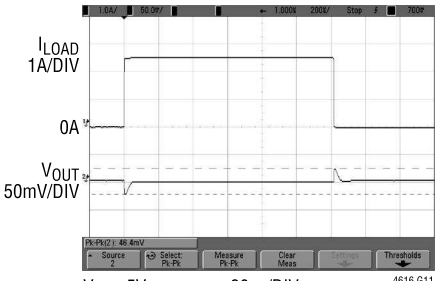
TYPICAL PERFORMANCE CHARACTERISTICS Specified as Each Channel

Load Transient Response



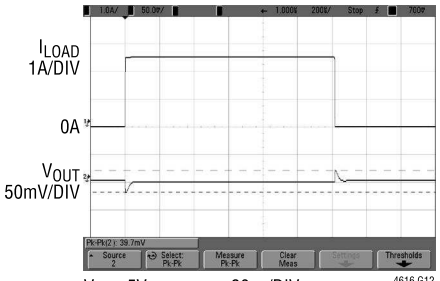
V_{IN} = 5V 20µs/DIV
V_{OUT} = 1.8V
2.5A/µs STEP
C_{OUT} = 2 × 100µF X5R, 470µF 4V POSCAP

Load Transient Response



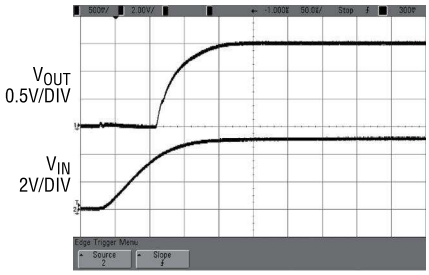
V_{IN} = 5V 20µs/DIV
V_{OUT} = 1.5V
2.5A/µs STEP
C_{OUT} = 2 × 100µF X5R, 470µF 4V POSCAP

Load Transient Response



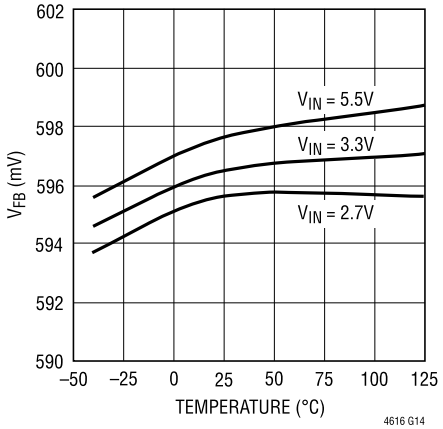
V_{IN} = 5V 20µs/DIV
V_{OUT} = 1.2V
2.5A/µs STEP
C_{OUT} = 2 × 100µF X5R, 470µF POSCAP

Start-Up

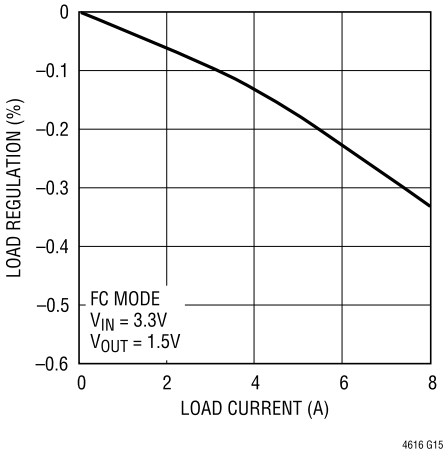


V_{IN} = 5V 50µs/DIV
V_{OUT} = 1.5V
C_{OUT} = 100µF NO LOAD AND 8A LOAD
(DEFAULT 100µs SOFT-START)

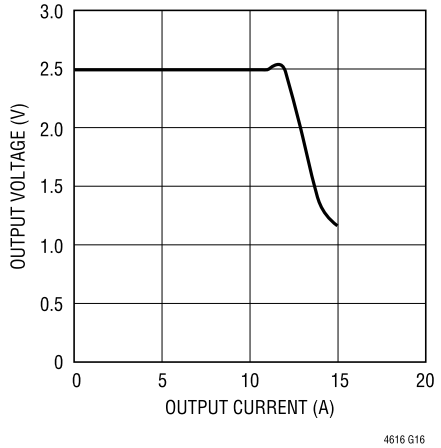
V_{FB} vs Temperature



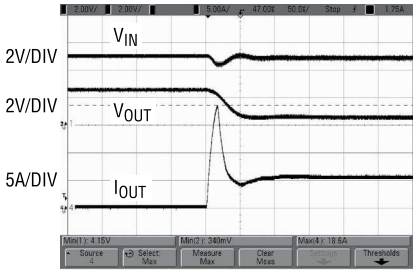
Load Regulation vs Current



2.5V Output Current

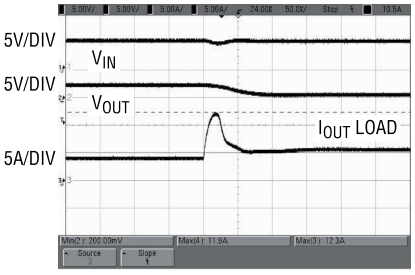


Short-Circuit Protection (2.5V Short, No Load)



V_{IN} = 5V 50µs/DIV
V_{OUT} = 2.5V

Short-Circuit Protection (2.5V Short, 4A Load)



V_{IN} = 5V 50µs/DIV
V_{OUT} = 2.5V

PIN FUNCTIONS

V_{IN1}, V_{IN2}, (BANK1 and BANK2); (F1-F4, E1-E4, C1-C2, D1-D2) and (J1-J2, K1-K2, L1-L4, M1-M4): Power Input Pins. Apply input voltage between these pins and GND pins. Recommend placing input decoupling capacitance directly between V_{IN} pins and GND pins.

V_{OUT1}, V_{OUT2} (BANK3 and BANK6); (D9-D12, E9-E12, F9-F12) and (K9-K12, L9-L12, M9-M12): Power Output Pins. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins. See Table 1.

GND1 and GND2 (BANK2 and BANK5); (A1-A5, A12, B1-B5, B7-B12, C3-C12, D3-D7) and (G1-G5, G12, H1-H5, H7-H12, J3-J12, K3-K7): Power Ground Pins for Both Input and Output Returns.

SV_{IN1} and SV_{IN2} (E5 and L5): Signal Input Voltage for Each Channel. This pin is internally connected to V_{IN} through a lowpass filter.

SGND1 and SGND2 (F5 and M5): Signal Ground Pin for Each Channel. Return ground path for all analog and low power circuitry. Tie a single connection to the output capacitor GND in the application. See layout guidelines in Figure 17.

MODE1 and MODE2 (A8 and G8): Mode Select Input for Each Channel. Tying this pin high enables Burst Mode operation. Tying this pin low enables forced continuous operation. Floating this pin or tying it to $V_{IN}/2$ enables pulse-skipping operation.

CLKIN1 and CLKIN2 (A7 and G7): External Synchronization Input to Phase Detector for Each Channel. This pin is internally terminated to SGND with a 50k resistor. The phase-locked loop will force the internal top power PMOS turn on to be synchronized with the rising edge of the CLKIN signal. Connect this pin to SV_{IN} to enable spread spectrum modulation. During external synchronization, make sure the PLLLPF pin is not tied to V_{IN} or GND.

PLLLPF1 and PLLLPF2 (E6 and L6): Phase-Locked Loop Lowpass Filter for Each Channel. An internal lowpass filter is tied to this pin. In spread spectrum mode, placing a capacitor here to SGND controls the slew rate from one frequency to the next. Alternatively, floating this pin allows normal running frequency at 1.5MHz, tying this pin to SV_{IN} forces the part to run at 1.33 times its normal frequency (2MHz), tying it to ground forces the frequency to run at 0.67 times its normal frequency (1MHz).

PHMODE1 and PHMODE2 (A9 and G9): Phase Selector Input for Each Channel. This pin determines the phase relationship between the internal oscillator and CLKOUT. Tie it high for 2-phase operation, tie it low for 3-phase operation, and float or tie it to $V_{IN}/2$ for 4-phase operation.

MGN1 and MGN2 (A10 and G10): Voltage Margining Pin for Each Channel. Increases or decreases the output voltage by the amount specified by the BSEL pin. To disable margining, tie the MGN pin to a voltage divider with 50k resistors from V_{IN} to ground (see Figure 5). For margining, connect a voltage divider from V_{IN} to GND with the center point connected to the MGN pin for the specific channel. Each resistor should be close to 50k. Margin High is within 0.3V of V_{IN}, and Margin Low is within 0.3V of GND. See the Applications Information section and Figure 18 for margining control. The specified tri-state drivers are capable of the high and low requirements for margining.

BSEL1 and BSEL2 (A6 and G6): Margining Bit Select Pin for Each Channel. Tying BSEL low selects ±5% margin value, tying it high selects 10% margin value. Floating it or tying it to $V_{IN}/2$ selects 15% margin value.

TRACK1 and TRACK2 (E8 and L8): Output Voltage Tracking Pin for Each Channel. Voltage tracking is enabled when the TRACK voltage is below 0.57V. If tracking is not desired, then connect the TRACK pin to SV_{IN}. If TRACK is not tied to SV_{IN}, then the TRACK pin's voltage needs to be below 0.18V before the chip shuts down even though RUN is

PIN FUNCTIONS

already low. Do not float this pin. A resistor and capacitor can be applied to the TRACK pin to increase the soft-start time of the regulator. TRACK1 and TRACK2 can be tied together for parallel operation and tracking. See the Applications Information section.

FB1 and FB2 (D8 and K8): The Negative Input of the Error Amplifier for Each Channel. Internally, this pin is connected to V_{OUT} with a 10k precision resistor. Different output voltages can be programmed with an additional resistor between FB and GND pins. In PolyPhase® operation, tying the FB pins together allows for parallel operation. See the Applications Information section for details.

I_{TH1} and I_{TH2} (F8 and M8): Current Control Threshold and Error Amplifier Compensation Point for Each Channel. The current comparator threshold increases with this control voltage. Tie together in parallel operation.

I_{THM1} and I_{THM2} (E7 and L7): Negative Input to the Internal I_{TH} Differential Amplifier for Each Channel. Tie this pin to SGND for single phase operation on each channel. For PolyPhase operation, tie the master's I_{THM} to SGND while connecting all of the I_{THM} pins together at the master.

PGOOD1 and PGOOD2 (A11 and G11): Output Voltage Power Good Indicator for Each Channel. Open-drain logic output that is pulled to ground when the output voltage is not within ±10% of the regulation point. Power good is disabled during margining.

RUN1 and RUN2 (F6 and M6): Run Control Pin. A voltage above 1.7V will turn on the module.

SW1 and SW2 (B6 and H6): Switching Node of Each Channel That is Used for Testing Purposes. This can be connected to an electronically open circuit copper pad on the board for improved thermal performance.

CLKOUT1 and CLKOUT2 (F7 and M7): Output Clock Signal for PolyPhase Operation. The phase of CLKOUT is determined by the state of the PHMODE pin.

SIMPLIFIED BLOCK DIAGRAM

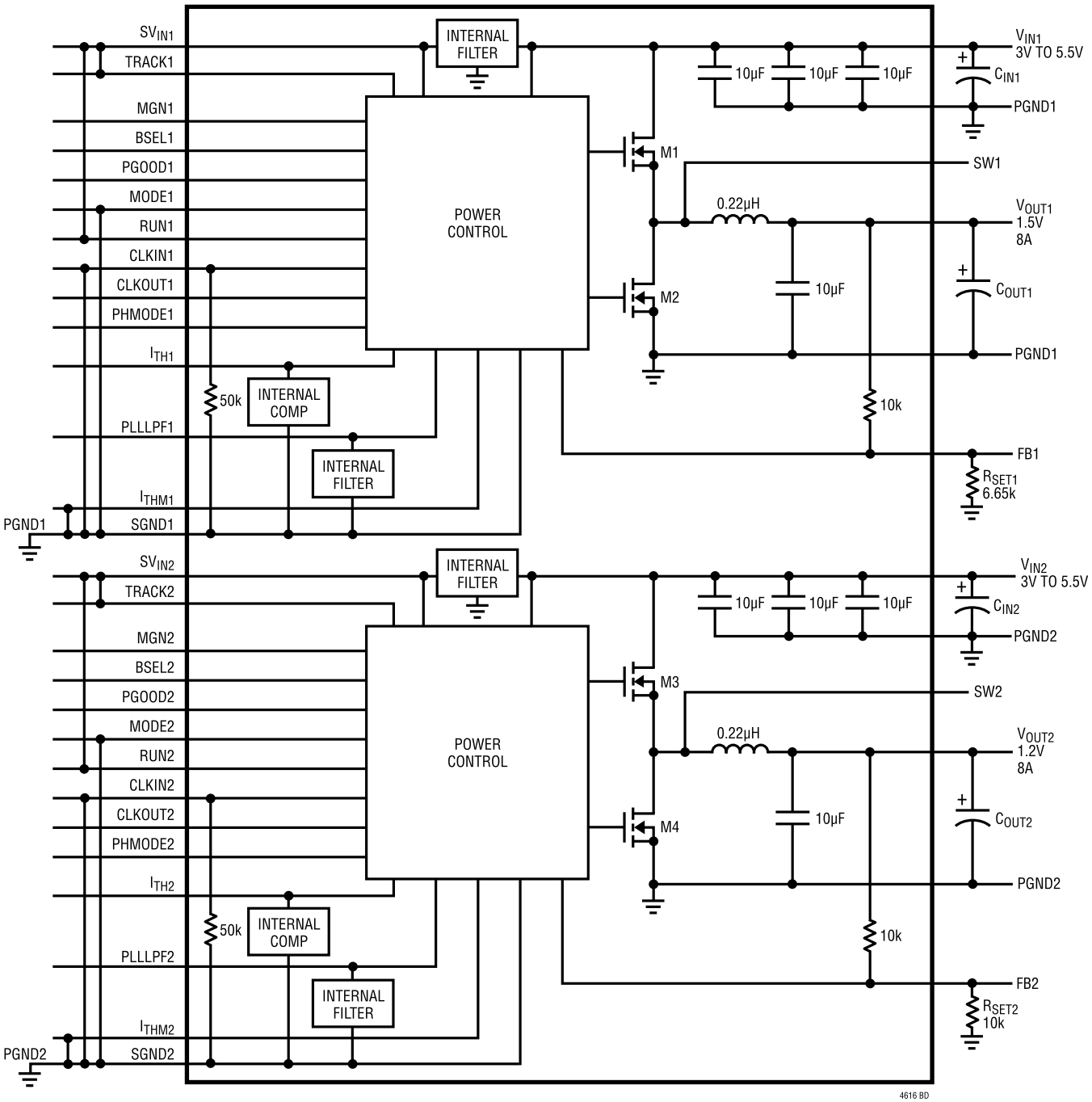


Figure 1. Simplified LTM4616 Block Diagram

SIMPLIFIED BLOCK DIAGRAM

Table 1. Decoupling Requirements. T_A = 25°C, Block Diagram Configuration.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN1} C_{IN2}	External Input Capacitor Requirement (V_{IN1} = 2.7V to 5.5V, V_{OUT1} = 1.5V) (V_{IN2} = 2.7V to 5.5V, V_{OUT2} = 2.5V)	 I_{OUT1} = 8A I_{OUT2} = 8A		 22 22		 µF µF
C_{OUT1} C_{OUT2}	External Output Capacitor Requirement (V_{IN1} = 2.7V to 5.5V, V_{OUT1} = 1.5V) (V_{IN2} = 2.7V to 5.5V, V_{OUT2} = 2.5V)	 I_{OUT1} = 8A I_{OUT2} = 8A		 100 100		 µF µF

OPERATION

The LTM4616 is a dual-output standalone nonisolated switching mode DC/DC power supply. It can provide two 8A outputs with few external input and output capacitors. This module provides precisely regulated output voltages programmable via external resistors from $0.6V_{DC}$ to $5V_{DC}$ over 2.7V to 5.5V input voltages. The typical application schematic is shown in Figure 18.

The LTM4616 has integrated constant frequency current mode regulators and built-in power MOSFET devices with fast switching speed. The typical switching frequency is 1.5MHz. For switching noise sensitive applications, it can be externally synchronized from 0.75MHz to 2.25MHz. Even spread spectrum switching can be implemented in the design to reduce noise.

With current mode control and internal feedback loop compensation, the LTM4616 module has sufficient stability margins and good transient performance with a wide range of output capacitors, even with all ceramic output capacitors.

Current mode control provides cycle-by-cycle fast current limit and thermal shutdown in an overcurrent condition. Internal overvoltage and undervoltage comparators pull the open-drain PGOOD output low if the output feedback voltage exits a ±10% window around the regulation point. The power good pins are disabled during margining.

Pulling the RUN pins below 1.3V forces the regulators into a shutdown state, by turning off both MOSFETs. The TRACK pin is used for programming the output voltage ramp and voltage tracking during start-up. See the Applications Information section.

The LTM4616 is internally compensated to be stable over all operating conditions. Table 3 provides a guideline for input and output capacitances for several operating conditions. LTpowerCAD™ design tool is available for fine tuning transient and stability performance. The FB pin is used to program the output voltage with a single external resistor to ground.

Multiphase operation can be easily employed with the synchronization and phase mode controls. The LTM4616 has clock in and clock out for poly phasing multiple devices or frequency synchronization.

High efficiency at light loads can be accomplished with selectable Burst Mode operation using the MODE pin. These light load features will accommodate battery operation. Efficiency graphs are provided for light load operation in the Typical Performance Characteristics section.

Output voltage margining is supported, and can be programed from ±5% to ±15% using the MGN and BSEL pins.