Am29LV800B

Data Sheet

RETIRED PRODUCT

This product has been retired and is not recommended for designs. For new and current designs, S29AL008D supersedes Am29LV800B and is the factory-recommended migration path. Please refer to the S29AL008D datasheet for specifications and ordering information. Availability of this document is retained for reference and historical purposes only.

July 2003

The following document specifies Spansion memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this datasheet as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal datasheet improvement and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about Spansion memory solutions.

Publication Number 21490 **Revision** G **Amendment** 5 **Issue Date** May 25, 2005

Am29LV800B

8 Megabit (1 M x 8-Bit/512 K x 16-Bit) CMOS 3.0 Volt-only Boot Sector Flash Memory

This product has been retired and is not recommended for designs. For new and current designs, S29AL008D supersedes Am29LV800B and is the factory-recommended migration path. Please refer to the S29AL008D datasheet for specifications and ordering information. Availability of this document is retained for reference and historical purposes only.

DISTINCTIVE CHARACTERISTICS

- **Single power supply operation**
  - 2.7 to 3.6 volt read and write operations for battery-powered applications
- **Manufactured on 0.32 µm process technology**
  - Compatible with 0.5 µm Am29LV800 device
- **High performance**
  - Access times as fast as 70 ns
- **Ultra low power consumption (typical values at 5 MHz)**
  - 200 nA Automatic Sleep mode current
  - 200 nA standby mode current
  - 7 mA read current
  - 15 mA program/e+5rase current
- **Flexible sector architecture**
  - One 16 Kbyte, two 8 Kbyte, one 32 Kbyte, and fifteen 64 Kbyte sectors (byte mode)
  - One 8 Kword, two 4 Kword, one 16 Kword, and fifteen 32 Kword sectors (word mode)
  - Supports full chip erase
  - Sector Protection features:

    A hardware method of locking a sector to prevent any program or erase operations within that sector

    Sectors can be locked in-system or via programming equipment

    Temporary Sector Unprotect feature allows code changes in previously locked sectors
- **Unlock Bypass Program Command**
  - Reduces overall programming time when issuing multiple program command sequences
- **Top or bottom boot block configurations available**
- **Embedded Algorithms**
  - Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
  - Embedded Program algorithm automatically writes and verifies data at specified addresses
- **Minimum 1 million write cycle guarantee per sector**
- **20-year data retention at 125°C**
  - Reliable operation for the life of the system
- **Package option**
  - 48-ball FBGA
  - 48-pin TSOP
  - 44-pin SO
  - Known Good Die (KGD) (see publication number 21536)
- **Compatibility with JEDEC standards**
  - Pinout and software compatible with single-power supply Flash
  - Superior inadvertent write protection
- **Data# Polling and toggle bits**
  - Provides a software method of detecting program or erase operation completion
- **Ready/Busy# pin (RY/BY#)**
  - Provides a hardware method of detecting program or erase cycle completion
- **Erase Suspend/Erase Resume**
  - Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Hardware reset pin (RESET#)**
  - Hardware method to reset the device to reading array data

Publication# **21490** Rev: **G** Amendment/**+5**
Issue Date: **May 25, 2005**

GENERAL DESCRIPTION

The Am29LV800B is an 8 Mbit, 3.0 volt-only Flash memory organized as 1,048,576 bytes or 524,288 words. The device is offered in 48-ball FBGA, 44-pin SO, and 48-pin TSOP packages. The device is also available in Known Good Die (KGD) form. For more information, refer to publication number 21536. The word-wide data (x16) appears on DQ15–DQ0; the byte-wide (x8) data appears on DQ7–DQ0. This device requires only a single, 3.0 volt V_{CC} supply to perform read, program, and erase operations. A standard EPROM programmer can also be used to program and erase the device.

This device is manufactured using AMD's 0.32 µm process technology, and offers all the features and benefits of the Am29LV800, which was manufactured using 0.5 µm process technology. In addition, the Am29LV800B features unlock bypass programming and in-system sector protection/unprotection.

The standard device offers access times of 70, 90, and 120 ns, allowing high speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

The device requires only a **single 3.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The **Unlock Bypass** mode facilitates faster programming times by requiring only two write cycles to program data instead of four.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both these modes.

AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

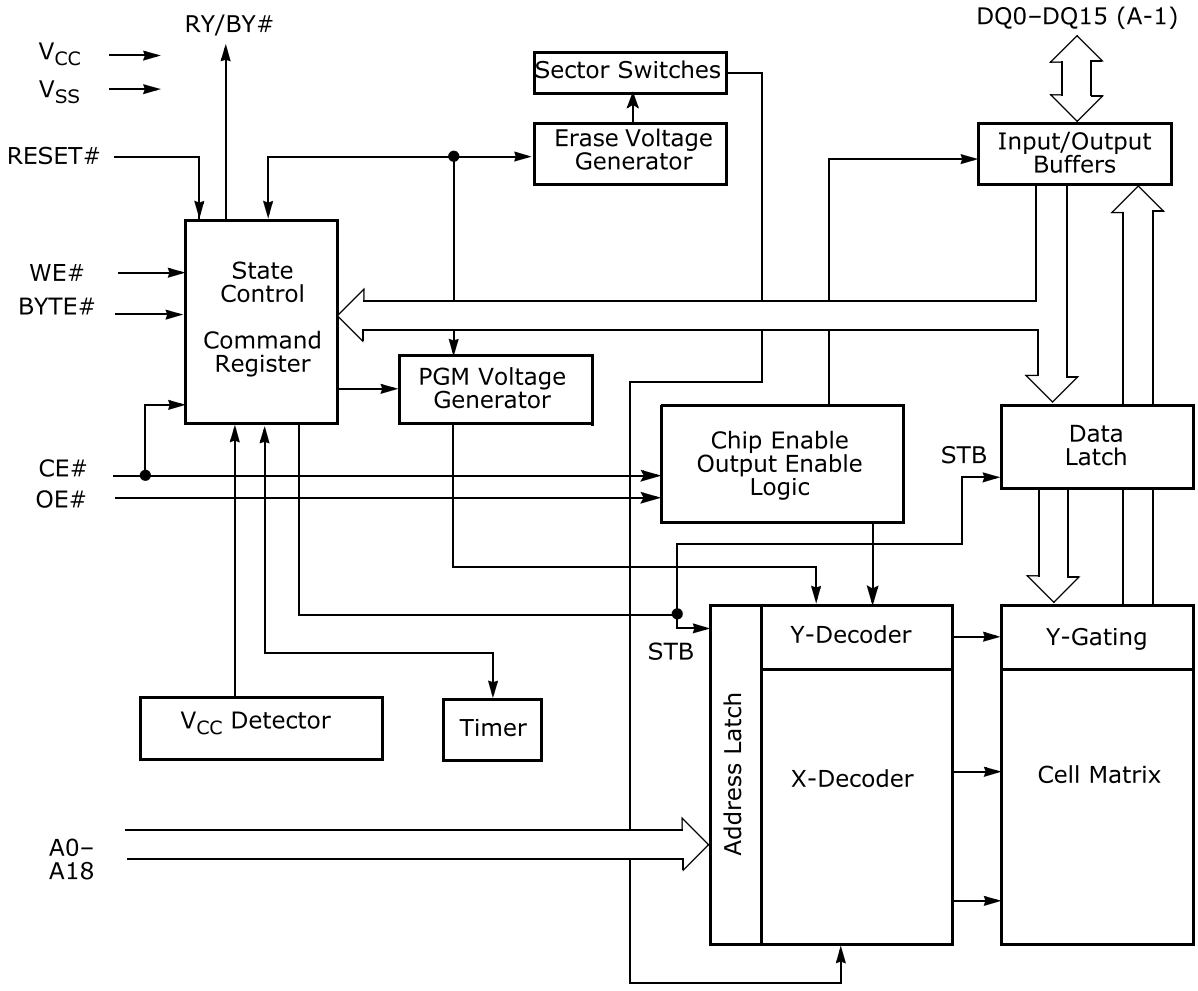
TABLE OF CONTENTS

PRODUCT SELECTOR GUIDE

Family Part Number		Am29LV800B		
Speed Options	Full Voltage Range: V_{CC} = 2.7–3.6 V	-70	-90	-120
Max access time, ns (t_{ACC})		70	90	120
Max CE# access time, ns (t_{CE})		70	90	120
Max OE# access time, ns (t_{OE})		30	35	50

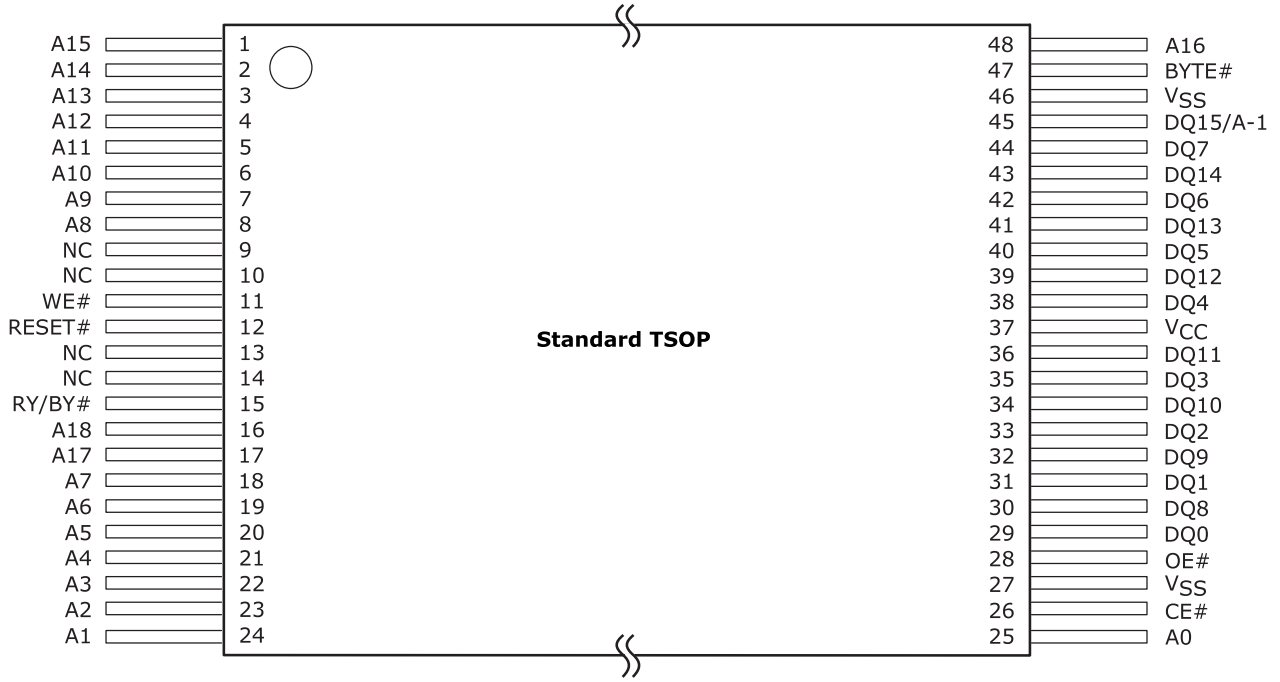
Note: *See "AC Characteristics" for full specifications.*

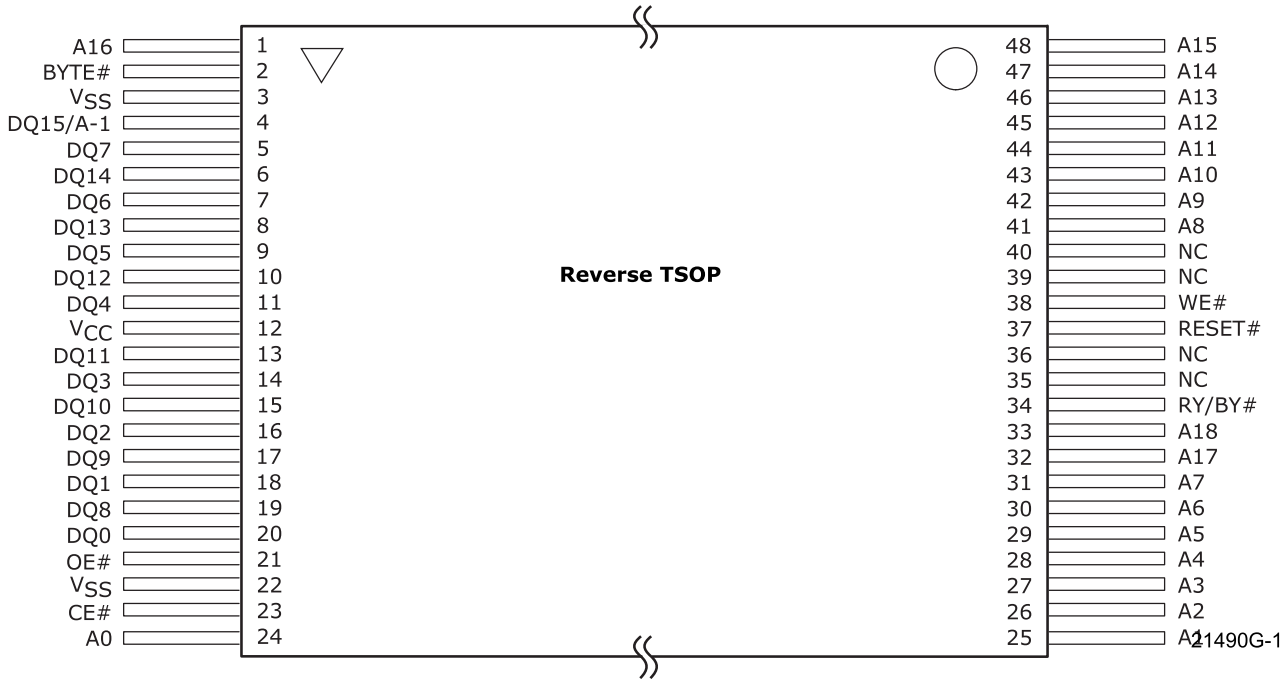
BLOCK DIAGRAM



CONNECTION DIAGRAMS

This device is also available in Known Good Die (KGD) form. Refer to publication number 21536 for more information.





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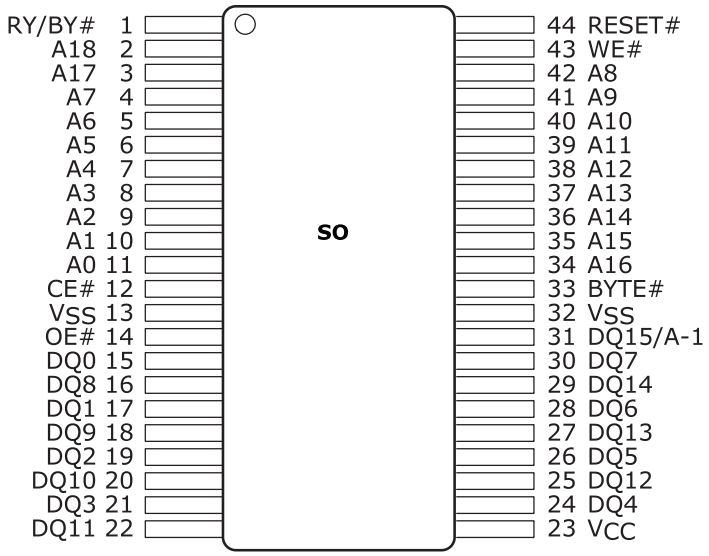


FBGA
Top View, Balls Facing Down

A6 A13	B6 A12	C6 A14	D6 A15	E6 A16	F6 BYTE#	G6 DQ15/A-1	H6 V_{SS}
A5 A9	B5 A8	C5 A10	D5 A11	E5 DQ7	F5 DQ14	G5 DQ13	H5 DQ6
A4 WE#	B4 RESET#	C4 NC	D4 NC	E4 DQ5	F4 DQ12	G4 V_{CC}	H4 DQ4
A3 RY/BY#	B3 NC	C3 A18	D3 NC	E3 DQ2	F3 DQ10	G3 DQ11	H3 DQ3
A2 A7	B2 A17	C2 A6	D2 A5	E2 DQ0	F2 DQ8	G2 DQ9	H2 DQ1
A1 A3	B1 A4	C1 A2	D1 A1	E1 A0	F1 CE#	G1 OE#	H1 V_{SS}

Special Handling Instructions for FBGA Package

Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

PIN CONFIGURATION

A0–A18 = 19 addresses

DQ0–DQ14= 15 data inputs/outputs

DQ15/A-1 = DQ15 (data input/output, word mode),
A-1 (LSB address input, byte mode)

BYTE# = Selects 8-bit or 16-bit mode

CE# = Chip enable

OE# = Output enable

WE# = Write enable

RESET# = Hardware reset pin, active low

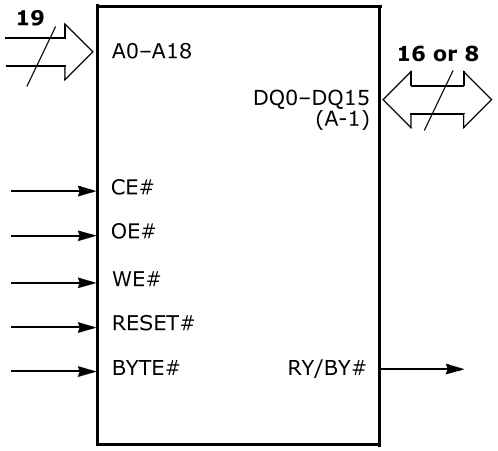
RY/BY# = Ready/Busy# output

V_{CC} = 3.0 volt-only single power supply (see Product Selector Guide for speed
options and voltage supply tolerances)

V_{SS} = Device ground

NC = Pin not connected internally

LOGIC SYMBOL



ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

Am29LV800B T -70 E C

TEMPERATURE RANGE

C = Commercial (0°C to +70°C)
D = Commercial (0°C to +70°C) with Pb-free package
I = Industrial (–40°C to +85°C)
F = Industrial (–40°C to +85°C) with Pb-free package
E = Extended (–55°C to +125°C)
K = Extended (–55°C to +125°C) with Pb-free package

PACKAGE TYPE

E = 48-Pin Thin Small Outline Package (TSOP) Standard Pinout (TS 048)
F = 48-Pin Thin Small Outline Package (TSOP) Reverse Pinout (TSR048)
S = 44-Pin Small Outline Package (SO 044)
WB = 48-Ball Fine Pitch Ball Grid Array (FBGA)
0.80 mm pitch, 6 x 9 mm package (FBB048)

This device is also available in Known Good Die (KGD) form. See publication number 21536 for more information.

SPEED OPTION

See Product Selector Guide and Valid Combinations

BOOT CODE SECTOR ARCHITECTURE

T = Top sector
B = Bottom sector

DEVICE NUMBER/DESCRIPTION

Am29LV800B
8 Megabit (1 M x 8-Bit/512 K x 16-Bit) CMOS Flash Memory
3.0 Volt-only Read, Program, and Erase

Valid Combinations for TSOP and SO Packages	
AM29LV800BT-70, AM29LV800BB-70	EC, EI, FC, FI, SC, SI, ED, EF, SD, SF
AM29LV800BT-90, AM29LV800BB-90	EC, EI, EE, ED, EF FC, FI, FE, SC, SI, SE, SD, SF, EK, SK
AM29LV800BT-120, AM29LV800BB-120	

Valid Combinations for FBGA Packages			
Order Number		**Package Marking**	
AM29LV800BT-70, AM29LV800BB-70	WBC, WBD, WBI, WBF	L800BT70V, L800BB70V	C, D, I, F
AM29LV800BT-90, AM29LV800BB-90	WBC, WBI, WBD, WBF, WBK, WBE	L800BT90V, L800BB90V	C, I, D, F K, E
AM29LV800BT-120, AM29LV800BB-120		L800BT12V, L800BB12V	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.