intel

28F256A
256K (32K x 8) CMOS FLASH MEMORY

- **Flash Electrical Chip-Erase**
  - **1 Second Typical Chip-Erase**
- **Quick-Pulse Programming Algorithm**
  - **10 μs Typical Byte-Program**
  - **0.5 Second Chip-Program**
- **100,000 Erase/Program Cycles**
- **12.0V ±5% V_{PP}**
- **High-Performance Read**
  - **120 ns Maximum Access Time**
- **CMOS Low Power Consumption**
  - **10 mA Typical Active Current**
  - **50 μA Typical Standby Current**
  - **0W Data Retention Power**
- **Integrated Program/Erase Stop Timer**
- **Command Register Architecture for Microprocessor/Microcontroller Compatible Write Interface**
- **Noise Immunity Features**
  - **± 10% V_{CC} Tolerance**
  - **Maximum Latch-Up Immunity through EPI Processing**
- **ETOX II Flash Nonvolatile Technology**
  - **EPROM-Compatible Process Base**
  - **High-Volume Manufacturing Experience**
- **JEDEC-Standard Pinouts**
  - **32-Pin PDIP**
  - **32-Lead PLCC**

  (See Packaging Spec., Order #231369)

Intel's 28F256A CMOS flash memory offers the most cost-effective and reliable alternative for read/write random access nonvolatile memory. The 28F256A adds electrical chip-erasure and reprogramming to familiar EPROM technology. Memory contents can be rewritten: in a test socket; in a PROM-programmer socket; on-board during subassembly test; in-system during final test; and in-system after-sale. The 28F256A increases memory flexibility, while contributing to time and cost savings.

The 28F256A is a 256-kilobit nonvolatile memory organized as 32,768 bytes of 8 bits. Intel's 28F256A is offered in 32-pin plastic dip and 32-lead PLCC. Pin assignments conform to JEDEC standards.

Extended erase and program cycling capability is designed into Intel's ETOX II (EPROM Tunnel Oxide) process technology. Advanced oxide processing, an optimized tunneling structure, and lower electric field combine to extend reliable cycling beyond that of traditional EEPROMs. With the 12.0V V_{PP} supply, the 28F256A performs a minimum of 10,000 erase and program cycles well within the time limits of the Quick-Pulse Programming and Quick-Erase algorithms.

Intel's 28F256A employs advanced CMOS circuitry for systems requiring high-performance access speeds, low power consumption, and immunity to noise. Its 120 ns access time provides no-WAIT-state performance for a wide range of microprocessors and microcontrollers. Typical standby current of 50 μA translates into power savings when the device is deselected. Finally, the highest degree of latch-up protection is achieved through Intel's unique EPI processing. Prevention of latch-up is provided for stresses up to 100 mA on address and data pins, from $-1V$ to $V_{CC} + 1V$.

With Intel's ETOX II process base, the 28F256A levers years of EPROM experience to yield the highest levels of quality, reliability, and cost-effectiveness.

October 1993
Order Number: 290243-006

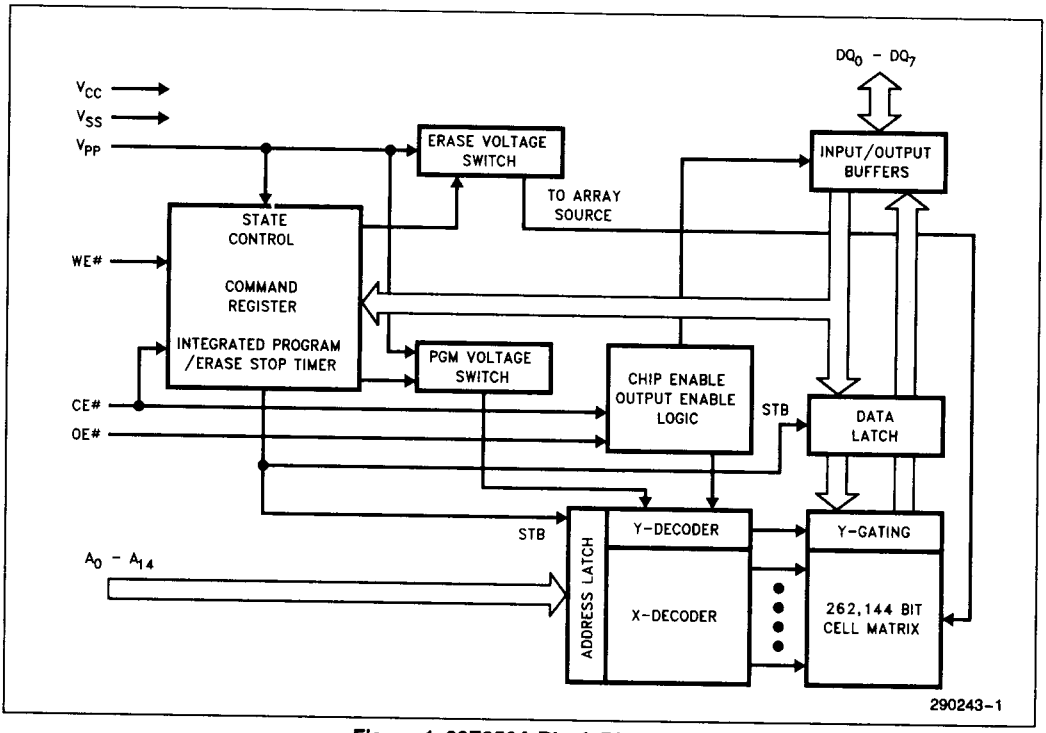

Figure 1. 28F256A Block Diagram

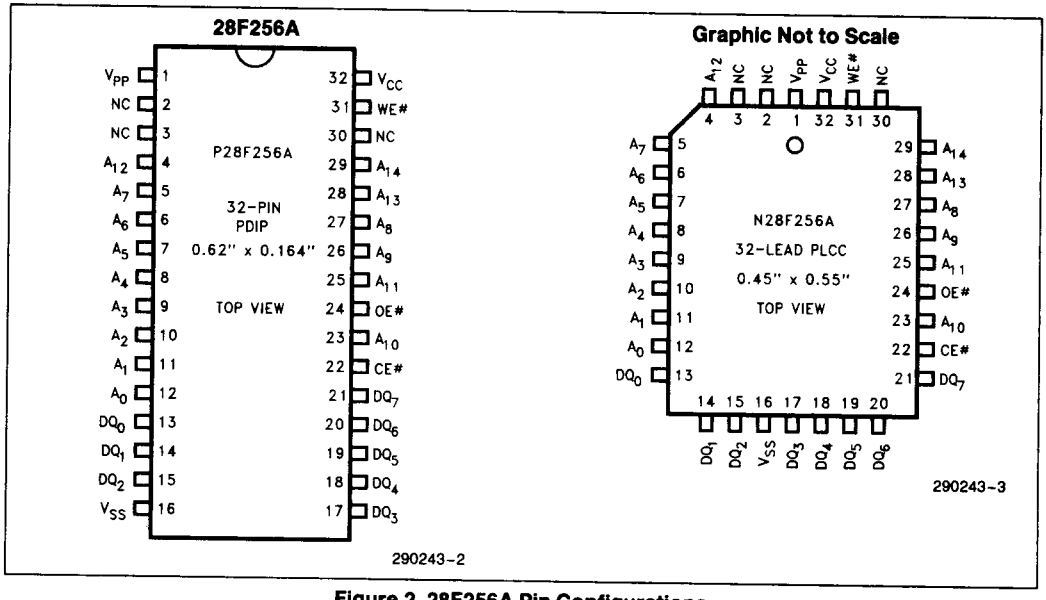

Figure 2. 28F256A Pin Configurations

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Table 1. Pin Description

Symbol	Type	Name and Function
A_0–A_{14}	INPUT	**ADDRESS INPUTS** for memory addresses. Addresses are internally latched during a write cycle.
DQ_0–DQ_7	INPUT/ OUTPUT	**DATA INPUT/OUTPUT:** Inputs data during memory write cycles; outputs data during memory read cycles. The data pins are active high and float to tri-state OFF when the chip is deselected or the outputs are disabled. Data is internally latched during a write cycle.
CE#	INPUT	**CHIP ENABLE** activates the device's control logic, input buffers, decoders, and sense amplifiers. CE# is active low; CE# high deselects the memory device and reduces power consumption to standby levels.
OE#	INPUT	**OUTPUT ENABLE** gates the devices output through the data buffers during a read cycle. OE# is active low.
WE#	INPUT	**WRITE ENABLE** controls writes to the control register and the array. Write enable is active low. Addresses are latched on the falling edge and data is latched on the rising edge of the WE# pulse. **Note:** With $V_{PP} \leq 6.5V$, memory contents cannot be altered.
V_{PP}		**ERASE/PROGRAM POWER SUPPLY** for writing the command register, erasing the entire array, or programming bytes in the array.
V_{CC}		**DEVICE POWER SUPPLY (5V ± 10%).**
V_{SS}		**GROUND.**
NC		**NO INTERNAL CONNECTION** to device. Pin may be driven or left floating.

APPLICATIONS

The 28F256A flash memory provides nonvolatility along with the capability to perform over 100,000 electrical chip-erasure/reprogram cycles. These features make the 28F256A an innovative alternative to disk, EEPROM, and battery-backed static RAM. Where periodic updates of code and data-tables are required, the 28F256A's reprogrammability and nonvolatility make it the obvious and ideal replacement for EPROM.

Primary applications and operating systems stored in flash eliminate the slow disk-DRAM download process. This results in a dramatic enhancement of performance and substantial reduction of power consumption—considerations particularly important in portable equipment. Flash memory increases flexibility with electrical chip-erasure and in-system update capability of operating systems and application code. With updatable BIOS, system manufacturers can easily accommodate last-minute changes as revisions are made.

In diskless workstations and terminals, network traffic reduces to a minimum and systems become instant-on. Reliability exceeds that of electromechanical media. Often in these environments, power interrupts force extended re-boot periods for all networked terminals. This mishap is no longer an issue if boot code, operating systems, communications protocols and primary applications are flash-resident in each terminal.

For embedded systems that rely on dynamic RAM/ disk for main system memory or nonvolatile backup storage, the 28F256A provides higher performance, lower power consumption, instant-on capability, and allows an "execute in place" memory hierarchy for code and data table reading. Additionally, the flash memory is more rugged and reliable in harsh environments where extreme temperatures and shock can cause disk-based systems to fail.

The need for code updates pervades all phases of a system's life—from prototyping to system manufacturing to after-sale service. The electrical chip-erasure and reprogramming ability of the 28F256A allows in-circuit alterability; this eliminates unnecessary handling and less-reliable socketed connections, while adding greater test, manufacture, and update flexibility.

Material and labor costs associated with code changes increases at higher levels of system inte-

gration—the most costly being code updates after sale. Code "bugs", or the desire to augment system functionality, prompt after-sale code updates. Field revision to EPROM-based code requires the removal of EPROM components or entire boards. With the 28F256A, code updates are implemented locally via an edge-connector, or remotely over a communications link.

For systems currently using a high-density static RAM/battery configuration for data accumulation, flash memory's inherent nonvolatility eliminates the need for battery backup. The concern for battery failure no longer exists, an important consideration for portable equipment and medical instruments, both requiring continuous performance. In addition, flash memory offers a considerable cost advantage over static RAM.

Flash memory's electrical chip-erasure, byte programmability and complete nonvolatility fit well with data accumulation and recording needs. Electrical chip-erasure gives the designer a "blank slate" in which to log or record data. Data can be periodically off-loaded for analysis and the flash memory erased producing a new "blank slate".

A high degree of on-chip feature integration simplifies memory-to-processor interfacing. Figure 3 depicts two 28F256As tied to the 80C186 system bus. The 28F256A's architecture minimizes interface circuitry needed for complete in-circuit updates of memory contents.

With cost-effective in-system reprogramming, extended cycling capability, and true nonvolatility, the 28F256A is a functional superset of one or more of the alternatives: EPROMs, EEPROMs, battery backed static RAM, or disk. EPROM-compatible read specifications, straightforward interfacing, and in-circuit alterability offer designers unlimited flexibility to meet the high standards of today's designs.

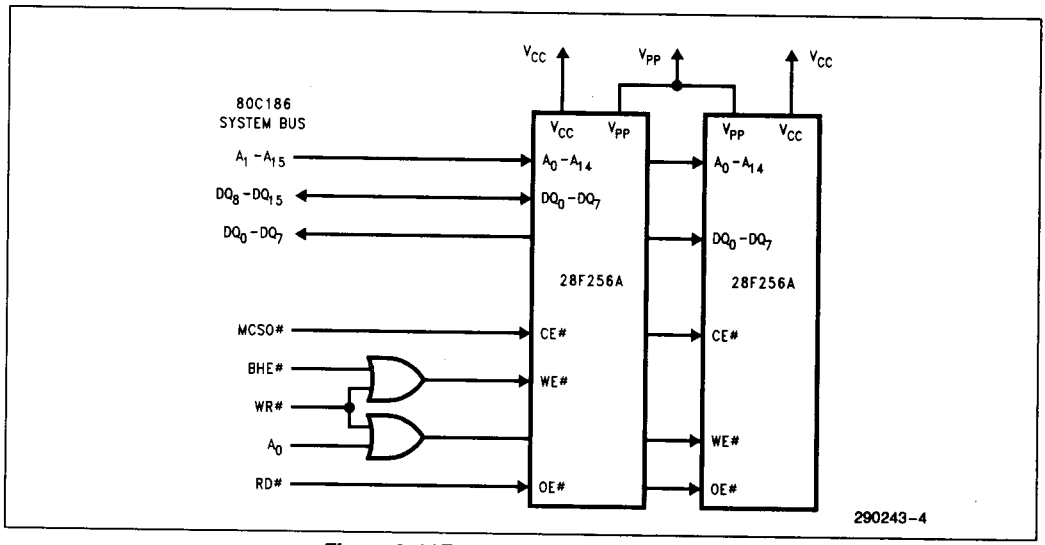

Figure 3. 28F256As in a 80C186 System

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PRINCIPLES OF OPERATION

Flash memory augments EPROM functionality with in-circuit electrical erasure and reprogramming. The 28F256A introduces a command register to manage this new functionality. The command register allows for: 100% TTL-level control inputs; fixed power supply during erasure and programming; and maximum EPROM compatibility.

In the absence of high voltage on the V_{PP} pin, the 28F256A is a read-only memory. Manipulation of the external memory-control pins yields the standard EPROM read, standby, output disable, and Intelligent Identifier operations.

The same EPROM read, standby, and output disable operations are available when high voltage is applied to the V_{PP} pin. In addition, high voltage on V_{PP} enables erasure and programming of the device. All functions associated with altering memory contents—Intelligent Identifier, erase, erase verify, program, and program verify—are accessed via the command register.

Commands are written to the register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which control the erase and programming circuitry. Write cycles also internally latch addresses and data needed for programming and erase operations. With the appropriate command written to the register, standard microprocessor read timings output array data, access the Intelligent Identifier codes, or output data for erase and program verification.

Integrated Program/Erase Stop Timer

Successive command write cycles define the duration of program and erase operations; specifically, the program or erase time durations are normally terminated by associated program or erase verify commands. An integrated stop timer provides simplified timing control over these operations; thus eliminating the need for maximum program/erase timing specifications. Programming and erase pulse durations are minimums only. When the stop timer terminates a program or erase operation, the device enters an inactive state and remains inactive until receiving the appropriate verify or reset command.

Write Protection

The command register is only active when V_{PP} is at high voltage. Depending upon the application, the system designer may choose to make the V_{PP} power supply switchable—available only when memory updates are desired. When $V_{PP} = V_{PPL}$, the contents of the register default to the read command, making the 28F256A a read-only memory. In this mode, the memory contents cannot be altered.

Or, the system designer may choose to "hardwire" V_{PP}, making the high voltage supply constantly available. In this case, all Command Register functions are inhibited whenever V_{CC} is below the write lockout voltage V_{LKO}. (See Power Up/Down Protection). The 28F256A is designed to accommodate either design practice, and to encourage optimization of the processor-memory interface.

The two-step program/erase write sequence to the Command Register provides additional software write protection.

BUS OPERATIONS

Read

The 28F256A has two control functions, both of which must be logically active, to obtain data at the outputs. Chip-Enable (CE#) is the power control and should be used for device selection. Output-Enable (OE#) is the output control and should be used to gate data from the output pins, independent of device selection. Refer to AC read timing waveforms.

When V_{PP} is high (V_{PPH}), the read operations can be used to access array data, to output the Intelligent Identifier codes, and to access data for program/erase verification. When V_{PP} is low (V_{PPL}), the read operation can access only the array data.

Output Disable

With Output-Enable at a logic-high level (V_{IH}), output from the device is disabled. Output pins are placed in a high-impedance state.

Standby

With Chip-Enable at a logic-high level, the standby operation disables most of the 28F256A's circuitry and substantially reduces device power consumption. The outputs are placed in a high-impedance

state, independent of the Output-Enable signal. If the 28F256A is deselected during erasure, programming, or program/erase verification, the device draws active current until the operation is terminated.

Intelligent Identifier Operation

The Intelligent Identifier operation outputs the manufacturer code (89H) and device code (B9H). Programming equipment automatically matches the device with its proper erase and programming algorithms. With Chip-Enable and Output-Enable at a logic low level, rising A_9 to high voltage V_{ID} (see D.C. Characteristics) activates the operation. Data read from locations 0000H and 0001H represent the manufacturer's code and the device code, respectively.

The manufacturer- and device-codes can also be read via the command register, for instances where the 28F256A is erased and reprogrammed in the target system. Following a write of 90H to the command register, a read from address location 0000H outputs the manufacturer code (89H). A read from address 0001H outputs the device code (B9H).

Write

Device erasure and programming are accomplished via the command register, when high voltage is applied to the V_{PP} pin. The contents of the register serve as input to the internal state-machine. The state-machine outputs dictate the function of the device.

The command register itself does not occupy an addressable memory location. The register is a latch used to store the command, along with address and data information needed to execute the command.

The command register is written by bringing Write-Enable to a logic-low level (V_{IL}), while Chip-Enable is low. Addresses are latched on the falling edge of Write-Enable, while data is latched on the rising edge of the Write-Enable pulse. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

COMMAND DEFINITIONS

When low voltage is applied to the V_{PP} pin, the contents of the command register default to 00H, enabling read-only operations.

Placing high voltage on the V_{PP} pin enables read/write operations. Device operations are selected by writing specific data patterns into the command register. Table 3 defines these 28F256A register commands.

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Table 2. 28F256A Bus Operations

	Pins / Operation	V_{PP}(1)	A_0	A_9	CE#	OE#	WE#	DQ_0–DQ_7
READ-ONLY	Read	V_{PPL}	A_0	A_9	V_{IL}	V_{IL}	V_{IH}	Data Out
	Output Disable	V_{PPL}	X(7)	X	V_{IL}	V_{IH}	V_{IH}	Tri-State
	Standby	V_{PPL}	X	X	V_{IH}	X	X	Tri-State
	Intelligent ID Manufacturer(2)	V_{PPL}	V_{IL}	V_{ID}(3)	V_{IL}	V_{IL}	V_{IH}	Data = 89H
	Intelligent ID Device(2)	V_{PPL}	V_{IH}	V_{ID}(3)	V_{IL}	V_{IL}	V_{IH}	Data = B9H
READ/WRITE	Read	V_{PPH}	A_0	A_9	V_{IL}	V_{IL}	V_{IH}	Data Out(4)
	Output Disable	V_{PPH}	X	X	V_{IL}	V_{IH}	V_{IH}	Tri-State
	Standby(5)	V_{PPH}	X	X	V_{IH}	X	X	Tri-State
	Write	V_{PPH}	A_0	A_9	V_{IL}	V_{IH}	V_{IL}	Data In (6)

NOTES:
1. Refer to DC Characteristics. When $V_{PP} = V_{PPL}$ memory contents can be read but not written or erased.
2. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 3. All other addresses low.
3. V_{ID} is the Intelligent Identifier high voltage. Refer to D.C. Characteristics.
4. Read operations with $V_{PP} = V_{PPH}$ may access array data or the Intelligent Identifier codes.
5. With V_{PP} at high voltage, the standby current equals $I_{CC} + I_{PP}$ (standby).
6. Refer to Table 3 for valid Data-In during a write operation.
7. X can be V_{IL} or V_{IH}.

Table 3. Command Definitions

Command	Bus Cycles Req'd	First Bus Cycle			Second Bus Cycle		
		Operation(1)	Address(2)	Data(3)	Operation(1)	Address(2)	Data(3)
Read Memory	1	Write	X	00H			
Read Intelligent ID Codes	3	Write	X	90H	Read	(4)	(4)
Set-Up Erase/Erase(6)	2	Write	X	20H	Write	X	20H
Erase Verify(6)	2	Write	EA	A0H	Read	X	EVD
Set-Up Program/Program(5)	2	Write	X	40H	Write	PA	PD
Program Verify(5)	2	Write	X	C0H	Read	X	PVD
Reset(7)	2	Write	X	FFH	Write	X	FFH

NOTES:
1. Bus operation are defined in Table 2.
2. IA = Identifier address: 00H for manufacturer code, 01H for device code.
   EA = Address of memory location to be read during erase verify.
   PA = Address of memory location to be programmed.
   Addresses are latched on the falling edge of the Write-Enable pulse.
3. ID = Data read from location IA during device identification. (Mfr = 89H, Device = B9H).
   EVD = Data read from location EA during erase verify.
   PD = Data to be programmed at location PA. Data is latched on the rising edge of the Write-Enable.
   PVD = Data read from location PA during program verify. PA is latched on the Program command.
4. Following the Read Intelligent ID command, two read operations access manufacturer and device codes.
5. Figure 4 illustrates the Quick-Pulse Programming Algorithm.
6. Figure 5 illustrates the Quick-Erase Algorithm.
7. The second bus cycle must be followed by the desired command register write.

Read Command

While V_{PP} is high, for erasure and programming, memory contents can be accessed via the read command. The read operation is initiated by writing 00H into the command register. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command register contents are altered.

The default contents of the register upon V_{PP} power-up is 00H. This default value ensures that no spurious alternation of memory contents occurs during the V_{PP} power transition. Where the V_{PP} supply is hard-wired to the 28F256A, the device powers-up and remains enabled for reads until the command register contents are changed. Refer to the AC Read Characteristics and Waveforms for specific timing parameters.

Intelligent Identifier Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer- and device-codes must be accessible while the device resides in the target system. PROM programmers typically access signature codes by raising A_9 to a high voltage. However, multiplexing high voltage onto address lines is not a desired system-design practice.

The 28F256A contains an Intelligent Identifier operation to supplement traditional PROM-programming methodology. The operation is initiated by writing 90H into the command register. Following the command write, a read cycle from address 0000H retrieves the manufacturer code 89H. A read cycle from address 0001H returns the device code B9H. To terminate the operation, it is necessary to write another valid command into the register.

Set-Up Erase/Erase Commands

Set-up Erase is a command-only operation that stages the device for electrical erase of all bytes in the array. The set-up erase operation is performed by writing 20H to the command register. To commence chip-erasure, the erase command (20H) must again be written to the register. The erase operation begins with the rising edge of the Write-Enable pulse and terminate with the rising edge of the next Write-Enable pulse (i.e., Erase-Verify Command).

This two-step sequence of set-up followed by execution ensures that memory contents are not accidentally erased. Also, chip-erasure can only occur when high voltage is applied to the V_{PP} pin. In the absence

of this high voltage, memory contents are protected against erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Erase-Verify Command

The erase command erases all of the bytes of the array in parallel. After each erase operation, all bytes must be verified. The erase verify operation is initiated by writing A0H into the command register. The address for the byte to be verified must be supplied as it is latched on the falling edge of the Write-Enable pulse. The register write terminates the erase operation with the rising edge of its Write-Enable pulse.

The 28F256A applies an internally-generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are erased.

The erase-verify command must be written to the command register prior to each byte verification to latch its address. The process continues for each byte in the array until a byte does not return FFH data, or the last address is accessed.

In the case where the data read is not FFH, another erase operation is performed. (Refer to Set-Up Erase/Erase.) Verification then resumes from the address of the last-verified byte. Once all bytes in the array have been verified, the erase step is complete. The device can be programmed. At this point, the verify operation is terminated by writing a valid command (e.g., Program Set-Up) to the command register. Figure 5, the Quick-Erase algorithm, illustrates how commands and bus operations are combined to perform electrical erasure of the 28F256A. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Set-Up Program/Program Commands

Set-up program is a command-only operation that stages the device for byte programming. Writing 40H into the command register performs the set-up operation.

Once the program set-up operation is performed, the next Write-Enable pulse causes a transition to an active programming operation. Addresses are internally latched on the falling edge of the Write-Enable pulse. Data is internally latched on the rising edge of the Write-Enable pulse. The rising edge of Write-Enable also begins the programming operation. The programming operation terminates with the next rising edge of Write-Enable, used to write the program-verify command. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Program Verify Command

The 28F256A is programmed on a byte-by-byte basis. Byte programming may occur sequentially or at random. Following each programming operation, the byte just programmed must be verified.

The program-verify operation is initiated by writing C0H into the command register. The register write terminates the programming operation with the rising edge of its Write-Enable pulse. The program-verify operation stages the device for verification of the byte last programmed. No new address information is latched.

The 28F256A applies an internally-generated margin voltage to the byte. A microprocessor read cycle outputs the data. A successful comparison between the programmed byte and true data means that the byte is successfully programmed. Programming then proceeds to the next desired byte location. Figure 4, the 28F256A Quick-Pulse Programming algorithm, illustrates how commands are combined with bus operations to perform byte programming. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Reset Command

A reset command is provided as a means to safely abort the erase- or program-command sequences. Following either set-up command (erase or program) with two consecutive writes of FFH will safely abort the operation. Memory contents will not be altered. A valid command must then be written to place the device in the desired state.

EXTENDED ERASE/PROGRAM CYCLING

EEPROM cycling failures have always concerned users. The high electrical field required by thin oxide EEPROMs for tunneling can literally tear apart the oxide at defect regions. To combat this, some suppliers have implemented redundancy schemes, reducing cycling failures to insignificant levels. However, redundancy requires that cell size be doubled—an expensive solution.

Intel has designed extended cycling capability into its ETOX II flash memory technology. Resulting improvements in cycling reliability come without increasing memory cell size or complexity. First, an

advanced tunnel oxide increases the charge carrying ability ten-fold. Second, the oxide area per cell subjected to the tunneling electric field is one-tenth that of common EEPROMs, minimizing the probability of oxide defects in the region. Finally, the peak electric field during erasure is approximately 2 MV/cm lower then EEPROM. The lower electric field greatly reduces oxide stress and the probability of failure—increasing time to wear out by a factor of 100,000,000.

The 28F256A is capable of 100,000 program/erase cycles. The device is programmed and erased using Intel's Quick-Pulse Programming and Quick-Erase algorithms. Intel's algorithmic approach uses a series of operations (pulses), along with byte verification, to completely and reliably erase and program the device.

For further reliability information, see Reliability Report RR-60 (ETOX II Reliability Data Summary).

QUICK-PULSE PROGRAMMING ALGORITHM

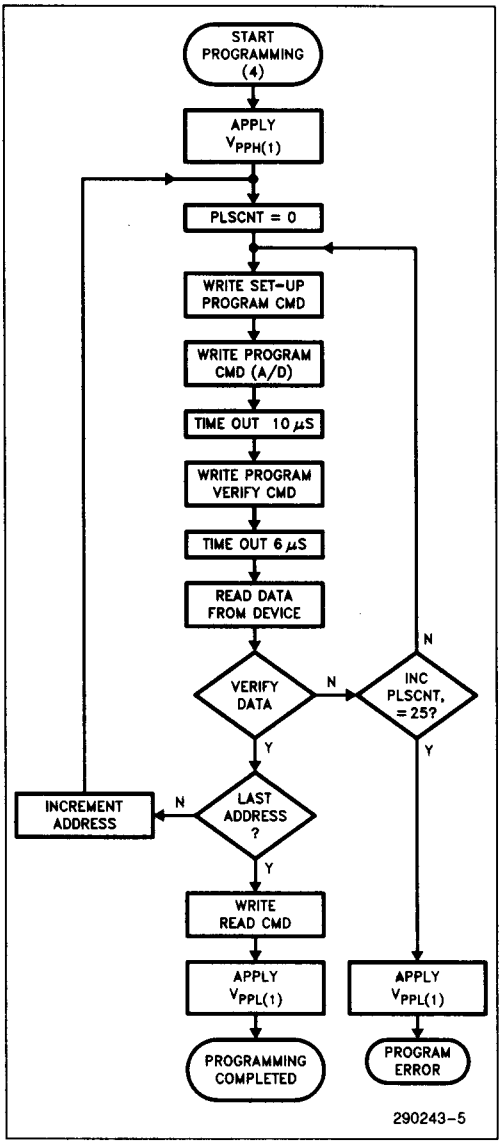
The Quick-Pulse Programming algorithm uses programming operations of 10 μs duration. Each operation is followed by a byte verification to determine when the addressed byte has been successfully programmed. The algorithm allows for up to 25 programming operations per byte, although most bytes verify on the first or second operation. The entire sequence of programming and byte verification is performed with V_{PP} at high voltage. Figure 4 illustrates the Quick-Pulse Programming algorithm.

QUICK-ERASE ALGORITHM

Intel's Quick-Erase algorithm yields fast and reliable electrical erasure of memory contents. The algorithm employs a closed-loop flow, similar to the Quick-Pulse Programming algorithm, to simultaneously remove charge from all bits in the array. Erasure begins with a read of memory contents. The 28F256A is erased when shipped from the factory. Reading FFH data from the device would immediately be followed by device programming.

For devices being erased and reprogrammed, uniform and reliable erasure is ensured by first programming all bits in the device to their charged state (data = 00H). This is accomplished, using the Quick-Pulse Programming algorithm, in approximately one-half second.

Erase execution then continues with an initial erase operation. Erase verification (data = FFH) begins at address 0000H and continues through the array to the last address, or until data other than FFH is encountered. With each erase operation, an increasing number of bytes verify to the erased state. Erase efficiency may be improved by storing the address of the last byte verified in a register. Following the next erase operation, verification starts at that stored address location. Erasure typically occurs in one second. Figure 5 illustrates the Quick-Erase algorithm.



Bus Operation	Command	Comments
Standby		Wait for V_{PP} ramp to V_{PPH} (= 12.0V) (1) Initialize pulse-count
Write	Set-Up Program	Data = 40H
Write	Program	Valid address/data
Standby		Duration of Program operation (t_{WHWH1})
Write	Program(2) Verify	Data = C0H; Stops (3) Program Operation
Standby		t_{WHGL}
Read		Read byte to verify programming
Standby		Compare data output to data expected
Write	Read	Data = 00H, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL}(1)

NOTES:
1. See DC Characteristics for the value of V_{PPH} and V_{PPL}.
2. Program Verify is only performed after byte programming. A final read/compare may be performed (optional) after the register is written with the Read command.
3. Refer to principles of operation.
4. CAUTION: The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

Figure 4. 28F256A Quick-Pulse Programming Algorithm

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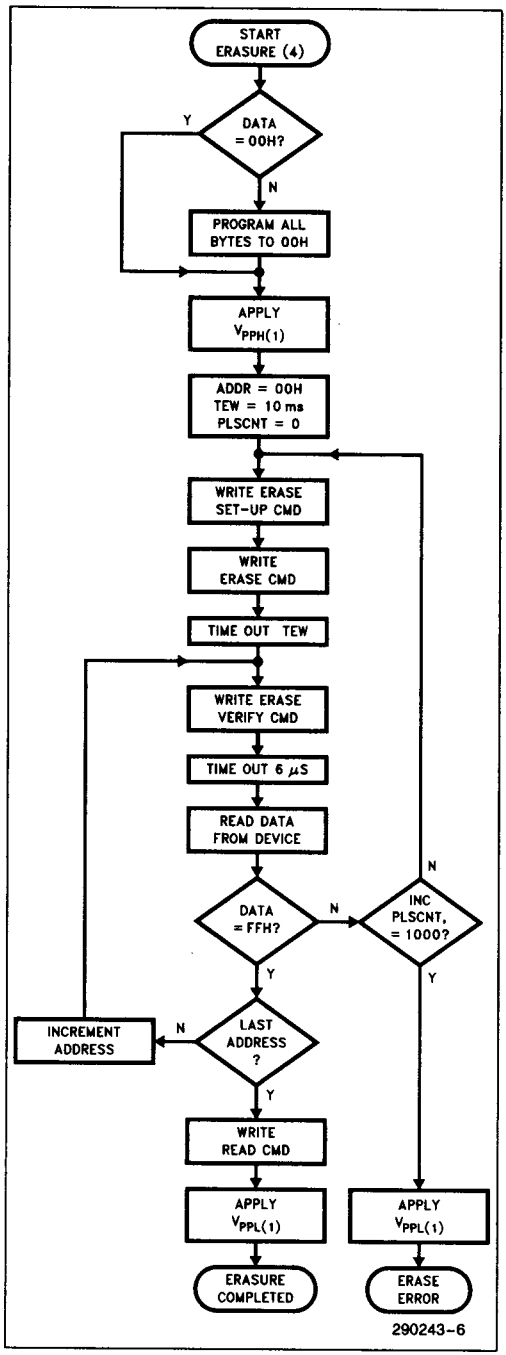

Bus Operation	Command	Comments
Standby		Wait for V_{PP} ramp to V_{PPH} (= 12.0V) (1) Use Quick-Pulse Programming (Fig. 4)
		Initialize Addresses, Erase Pulse Width, and Pulse Count
Write	Set-Up Erase	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase operation (t_{WHWH2})
Write	Erase Verify(2)	Addr = Byte to verify; Data = A0H; Stops Erase Operation (3)
Standby		t_{WHGL}
Read		Read byte to verify erasure
Standby		Compare output to FFH increment pulse count
Write	Read	Data = 00H, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL}(1)

NOTES:
1. See DC Characteristics for the value of V_{PPH} and V_{PPL}.
2. Erase Verify is performed only after chip-erasure. A final read/compare may be performed (optional) after the register is written with the Read command.
3. Refer to principles of operation.
4. CAUTION: The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.

Figure 5. 28F256A Quick-Erase Algorithm

DESIGN CONSIDERATIONS

Two-Line Output Control

Flash memories are often used in larger memory arrays. Intel provides two read-control inputs to accommodate multiple memory connections. Two-line control provides for:

a. the lowest possible memory power dissipation, and

b. complete assurance that output bus contention will not occur.

To efficiently use these two control units, an address-decoder output should drive chip-enable, while the system's read signal controls all flash memories and other parallel memories. This assures that only enabled memory devices have active outputs, while deselected devices maintain the low power standby condition.

Power Supply Decoupling

Flash memory power-switching characteristics require careful device decoupling. System designers are interested in three supply current (I_{CC}) issues—standby, active, and transient current peaks produced by falling and rising edges of chip-enable. The capacitive and inductive loads on the device outputs determine the magnitudes of these peaks.

Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 μF ceramic capacitor connected between V_{CC} and V_{SS}, and between V_{PP} and V_{SS}.

Place the high-frequency, low-inherent-inductance capacitors as close as possible to the devices. Also, for every eight devices, a 4.7 μF electrolytic capacitor should be placed at the array's power supply connection, between V_{CC} and V_{SS}. The bulk capacitor will overcome voltage slumps caused by printed-circuit-board trace inductance, and will supply charge to the smaller capacitors as needed.

V_{PP} Trace on Printed Circuit Boards

Programming flash memories, while they reside in the target smith, requires that the printed circuit board designer pay attention to the V_{PP} pin power supply trace. Use similar trace widths and layout considerations given the V_{CC} power bus. Adequate V_{PP} supply traces and decoupling will decrease V_{PP} voltage spikes and overshoots.

Power Up/Down Protection

The 28F256A is designed to offer protection against accidental erasure or programming during power transitions. Upon power-up, the 28F256A is indifferent as to which power supply, V_{PP} or V_{CC}, powers up first. **Power supply sequencing is not required.** Internal circuitry in the 28F256A ensures that the command register is reset to the read mode upon power up.

A system designer must guard against active writes for V_{CC} voltages above V_{LKO} when V_{PP} is active. Since both WE# and CE# must be low for a command write, driving either to V_{IH} will inhibit writes. The control register architecture provides an added level of protection since alteration of memory contents only occurs after successful completion of the two-step command sequences.

28F256A Power Dissipation

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash nonvolatility increases the usable battery life of your system because the 28F256A does not consume any power to retain code or data when the system is off. Table 4 illustrates the power dissipated when updating the 28F256A.

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Table 4. 28F256A Typical Update Power Dissipation(4)

Operation	Power Dissipation (Watt-Seconds)	Notes
Array Program/Program Verify	0.043	1
Array Erase/Erase Verify	0.083	2
One Complete Cycle	0.169	3

NOTES:
1. Formula to calculate typical Program/Program Verify Power = [V_{PP} × # Bytes × typical # Prog Pulses (t_{WHWH1} × I_{PP2} typical + t_{WHGL} × I_{PP4} typical)] + [V_{CC} × # Bytes × typical # Prog Pulses (t_{WHWH1} × I_{CC2} typical + t_{WHGL} × I_{CC4} typical)].
2. Formula to calculate typical Erase/Erase Verify Power = [V_{pp} (I_{PP3} typical × t_{ERASE} typical + I_{PP5} typical × t_{WHGL} × # Bytes)] + [V_{CC}(I_{CC3} typical × t_{ERASE} typical + I_{CC5} typical × t_{WHGL} × # Bytes)].
3. One Complete Cycle = Array Preprogram + Array Erase + Program.
4. "Typicals" are not guaranteed, but based on a limited number of samples from production lots.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
During Read .....0°C to +70°C(1)
During Erase/Program .....0°C to +70°C

Temperature Under Bias .....−10°C to +80°C

Storage Temperature .....−65°C to +125°C

Voltage on Any Pin with
Respect to Ground .....−2.0V to +7.0V(2)

Voltage on Pin A_9 with
Respect to Ground .....−2.0V to +13.5V(2, 3)

V_{PP} Supply Voltage with
Respect to Ground
During Erase/Program .....−2.0V to +14.0(2, 3)

V_{CC} Supply Voltage with
Respect to Ground .....−2.0V to +7.0V(2)

Output Short Circuit Current.....100 mA(4)

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

NOTES:
1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC input voltage is −0.5V. During transitions, inputs may undershoot to −2.0V for periods less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods less than 20 ns.
3. Maximum DC voltage on A_9 or V_{PP} may overshoot to +14.0V for periods less than 20 ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.

OPERATING CONDITIONS

Symbol	Parameter	Limits		Unit	Comments
		Min	Max		
T_A	Operating Temperature	0	70	°C	For Read-Only and Read/Write Operations
V_{CC}	V_{CC} Supply Voltage	4.50	5.50	V	

DC CHARACTERISTICS—TTL/NMOS COMPATIBLE

Symbol	Parameter	Notes	Limits			Unit	Test Conditions
			Min	Typical(4)	Max		
I_{LI}	Input Leakage Current	1			±1.0	μA	$V_{CC} = V_{CC}$ max $V_{IN} = V_{CC}$ or V_{SS}
I_{LO}	Output Leakage Current	1			±10.0	μA	$V_{CC} = V_{CC}$ max $V_{OUT} = V_{CC}$ or V_{SS}
I_{CCS}	V_{CC} Standby Current	1		0.3	1.0	mA	$V_{CC} = V_{CC}$max CE# = V_{IH}
I_{CC1}	V_{CC} Active Read Current	1		10	30	mA	$V_{CC} = V_{CC}$max CE# = V_{IL} f = 6 MHz, I_{OUT} = 0 mA
I_{CC2}	V_{CC} Programming Current	1, 2		1.0	10	mA	Programming in Progress
I_{CC3}	V_{CC} Erasure Current	1, 2		5.0	15	mA	Erasure in Progress
I_{CC4}	V_{CC} Program Verify Current	1, 2		5.0	15	mA	$V_{PP} = V_{PPH}$ Program Verify in Progress
I_{CC5}	V_{CC} Erase Verify Current	1, 2		5.0	15	mA	$V_{PP} = V_{PPH}$ Erase Verify in Progress
I_{PPS}	V_{PP} Leakage Current	1			±10.0	μA	$V_{PP} \leq V_{CC}$
I_{PP1}	V_{PP} Read Current, ID Current, or Standby Current	1		90	200	μA	$V_{PP} > V_{CC}$
					±10.0		$V_{PP} \leq V_{CC}$
I_{PP2}	V_{PP} Programming Current	1, 2		8.0	30	mA	$V_{PP} = V_{PPH}$ Programming in Progress
I_{PP3}	V_{PP} Erase Current	1, 2		4.0	20	mA	$V_{PP} = V_{PPH}$ Erasure in Progress
I_{PP4}	V_{PP} Program Verify Current	1, 2		2.0	5.0	mA	$V_{PP} = V_{PPH}$ Program Verify in Progress
I_{PP5}	V_{PP} Erase Verify Current	1, 2		2.0	5.0	mA	$V_{PP} = V_{PPH}$ Erase Verify in Progress
V_{IL}	Input Low Voltage		−0.5		0.8	V	
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage				0.45	V	I_{OL} = 5.8 mA $V_{CC} = V_{CC}$ min
V_{OH1}	Output High Voltage		2.4			V	I_{OH} = −2.5 mA $V_{CC} = V_{CC}$min
V_{ID}	A_9 Intelligent Identifier Voltage		11.50		13.00	V	
I_{ID}	A_9 Intelligent Identifier Current	1, 2		90	200	μA	$A_9 = V_{ID}$
V_{PPL}	V_{PP} During Read-Only Operations		0.00		6.5	V	Note: Erase/Program are Inhibited when $V_{PP} = V_{PPL}$
V_{PPH}	V_{PP} During Read/Write Operations		11.40		12.60	V	
V_{LKO}	V_{CC} Erase/Write Lock Voltage		2.5			V	

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DC CHARACTERISTICS—CMOS COMPATIBLE

Symbol	Parameter	Notes	Limits			Unit	Test Conditions
			Min	Typical(4)	Max		
I_{LI}	Input Leakage Current	1			±1.0	μA	$V_{CC} = V_{CC}$ max $V_{IN} = V_{CC}$ or V_{SS}
I_{LO}	Output Leakage Current	1			±10.0	μA	$V_{CC} = V_{CC}$ max $V_{OUT} = V_{CC}$ or V_{SS}
I_{CCS}	V_{CC} Standby Current	1		50	100	μA	$V_{CC} = V_{CC}$max CE# = V_{CC} ±0.2V
I_{CC1}	V_{CC} Active Read Current	1		10	30	mA	$V_{CC} = V_{CC}$max CE# = V_{IL} f = 6 MHz, I_{OUT} = 0 mA
I_{CC2}	V_{CC} Programming Current	1, 2		1.0	10	mA	Programming in Progress
I_{CC3}	V_{CC} Erase Current	1, 2		5.0	15	mA	Erasure in Progress
I_{CC4}	V_{CC} Program Verify Current	1, 2		5.0	15	mA	$V_{PP} = V_{PPH}$ Program Verify in Progress
I_{CC5}	V_{CC} Erase Verify Current	1, 2		5.0	15	mA	$V_{PP} = V_{PPH}$ Erase Verify in Progress
I_{PPS}	V_{PP} Leakage Current	1			±10.0	μA	$V_{PP} \leq V_{CC}$
I_{PP1}	V_{PP} Read Current, ID Current, or Standby Current	1		90	200	μA	$V_{PP} > V_{CC}$
					±10.0		$V_{PP} \leq V_{CC}$
I_{PP2}	V_{PP} Programming Current	1, 2		8.0	30	mA	$V_{PP} = V_{PPH}$ Programming in Progress
I_{PP3}	V_{PP} Erase Current	1, 2		4.0	20	mA	$V_{PP} = V_{PPH}$ Erasure in Progress
I_{PP4}	V_{PP} Program Verify Current	1, 2		2.0	5.0	mA	$V_{PP} = V_{PPH}$ Program Verify in Progress
I_{PP5}	V_{PP} Erase Verify Current	1, 2		2.0	5.0	mA	$V_{PP} = V_{PPH}$ Erase Verify in Progress
V_{IL}	Input Low Voltage		−0.5		0.8	V	
V_{IH}	Input High Voltage		0.7V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage				0.45	V	I_{OL} = 5.8 mA $V_{CC} = V_{CC}$ min
V_{OH1}	Output High Voltage		0.85V_{CC}			V	I_{OH} = −2.5 mA, $V_{CC} = V_{CC}$ min
V_{OH2}			V_{CC} −0.4				I_{OH} = 100 μA, $V_{CC} = V_{CC}$ min
V_{ID}	A_9 Intelligent Identifier Voltage		11.50		13.00	V	
I_{ID}	A_9 Intelligent Identifier Current	1, 2		90	200	μA	$A_9 = V_{ID}$

DC CHARACTERISTICS—CMOS COMPATIBLE (Continued)

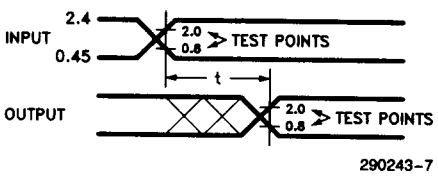
Symbol	Parameter	Notes	Limits			Unit	Test Conditions
			Min	Typical(4)	Max		
V_{PPL}	V_{PP} During Read-Only Operations		0.00		6.5	V	Note: Erase/Program are Inhibited when $V_{PP} = V_{PPL}$
V_{PPH}	V_{PP} During Read/Write Operations		11.40		12.60	V	
V_{LKO}	V_{CC} Erase/Write Lock Voltage		2.5			V	

CAPACITANCE(3) T = 25°C, f = 1.0 MHz

Symbol	Parameter	Notes	Limits		Unit	Conditions
			Min	Max		
C_{IN}	Address/Control Capacitance	3		6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	3		12	pF	$V_{OUT} = 0V$

NOTES FOR DC CHARACTERISTICS AND CAPACITANCE:
1. All currents are in RMS unless otherwise noted. Typical values at $V_{CC} = 5.0V$, $V_{PP} = 12.0V$, T = 25°C. These currents are valid for all product versions (Packages and Speeds).
2. Not 100% tested: characterization data available.
3. Sampled, not 100% tested.
4. "Typicals" are not guaranteed, but based on a limited number of samples from production lots.

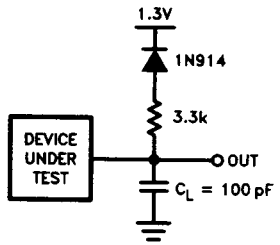
AC TESTING INPUT/OUTPUT WAVEFORM



290243-7

AC Testing: Inputs are driven at 2.5V for a logic "1" and 0.45 for a logic "0". Testing measurements are made at 2.0 for a logic "1" and 0.8 for a logic "0". Rise/Fall time ≤ 10 ns.

AC TESTING LOAD CIRCUIT



C_L = 100 pF
C_L includes Jig Capacitance

290243-8

AC Test Conditions

Input Rise and Fall Times (10% to 90%) ..... 10 ns
Input Pulse Levels ..... 0.45 and 2.4
Input Timing Reference Level ..... 0.8 and 2.0
Output Timing Reference Level ..... 0.8 and 2.0

AC CHARACTERISTICS Read-Only Operations

Versions		Notes	28F256A-120		28F256A-150		Unit
Symbol	Characteristic		Min	Max	Min	Max	
t_{AVAV}/t_{RC}	Read Cycle Time		120		150		ns
t_{ELQV}/t_{CE}	Chip Enable Access Time			120		150	ns
t_{AVQV}/t_{ACC}	Address Access Time			120		150	ns
t_{GLQV}/t_{OE}	Output Enable Access Time			50		55	ns
t_{ELQX}/t_{LZ}	Chip Enable to Output in Low Z	2, 3	0		0		ns
t_{EHQZ}	Chip Disable to Output in High Z	2		55		55	ns
t_{GLQX}/t_{OLZ}	Output Enable to Output in Low Z	2, 3	0		0		ns
t_{GHQZ}/t_{DF}	Output Disable to Output in High Z	2		30		35	ns
t_{OH}	Output Hold from Address, CE#, or OE# Change	1, 2	0		0		ns
t_{WHGL}	Write Recovery Time before Read		6		6		μs

NOTES:
1. Whichever occurs first.
2. Sampled, not 100% tested.
3. Guaranteed by design.

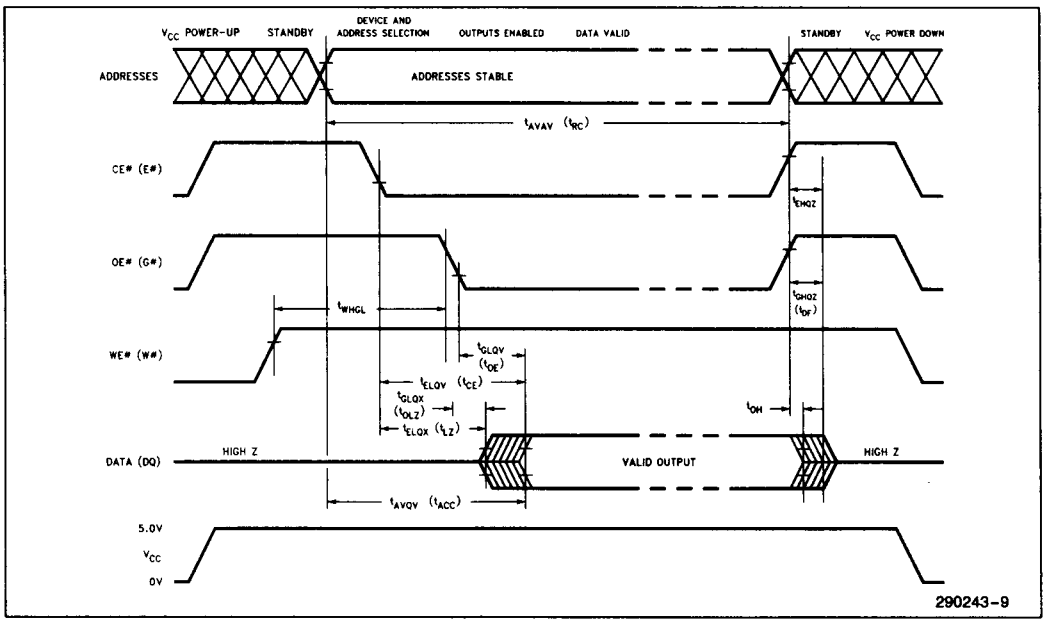


Figure 6. AC Waveform for Read Operations

AC CHARACTERISTICS—For Write/Erase/Program Operations(1)

Versions		Notes	28F256A-120		28F256A-150		Unit
Symbol	Characteristic		Min	Max	Min	Max	
t_{AVAV}/t_{WC}	Write Cycle Time		120		150		ns
t_{AVWL}/t_{AS}	Address Set-Up Time		0		0		ns
t_{WLAX}/t_{AH}	Address Hold Time		60		60		ns
t_{DVWH}/t_{DS}	Data Set-Up Time		50		50		ns
t_{WHDX}/t_{DH}	Data Hold Time		10		10		ns
t_{WHGL}	Write Recovery Time before Read		6		6		µs
t_{GHWL}	Read Recovery Time before Write	2	0		0		µs
t_{ELWL}/t_{CS}	Chip Enable Set-Up Time before Write		20		20		ns
t_{WHEH}/t_{CH}	Chip Enable Hold Time		0		0		ns
t_{WLWH}/t_{WP}	Write Pulse Width		60		60		ns
t_{WHWL}/t_{WPH}	Write Pulse Width High		20		20		ns
t_{WHWH1}	Duration of Programming Operation	3	10		10		µs
t_{WHWH2}	Duration of Erase Operation	3	9.5		9.5		ms
t_{VPEL}	V_{PP} Set-Up Time to Chip Enable Low	2	1.0		1.0		µs

NOTES:
1. Read timing parameters during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read-Only Operations.
2. Guaranteed by design.
3. The integrated stop timer terminates the programming/erase operations, thereby eliminating the need for a maximum specification.

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Notes	Limits						Unit
		28F256A-120			28F256A-150			
		Min	Typ	Max	Min	Typ	Max	
Chip Erase Time	1, 3, 4		1	10		1	10	sec
Chip Program Time	1, 2, 4		0.5	3		0.5	3	sec

NOTES:
1. "Typicals" are not guaranteed, but based on a limited number of samples taken from production lots. Data taken at 25°C, 12.0V V_{PP}, at 0 cycles.
2. Minimum byte programming time excluding system overhead is 16 µs program + 6 µs write recovery), while maximum is 400 µs/byte (16 µs x 25 loops allowed by algorithm). Max chip programming is specified lower than the worst case allowed by the programming algorithm since most bytes program significantly faster than the worst case byte.
3. Excludes 00H Programming Prior to Erasure.
4. Excludes System-Level Overhead.
5. Refer to RR-60 "ETOX" II Flash Memory Reliability Data Summary for typical cycling data and failure rate calculations.

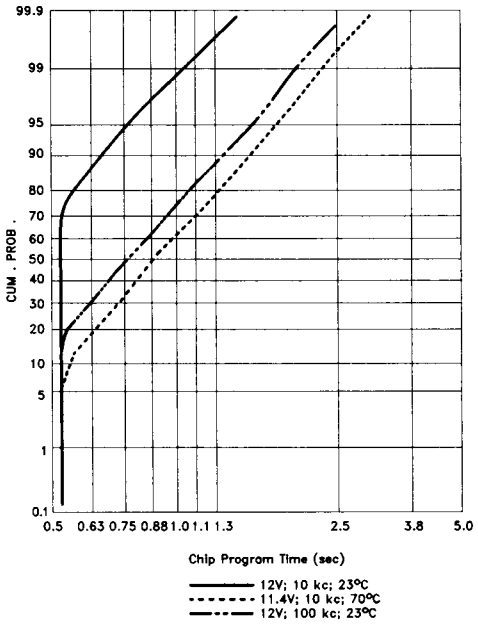


Figure 7. 28F256A Typical Programming Capability

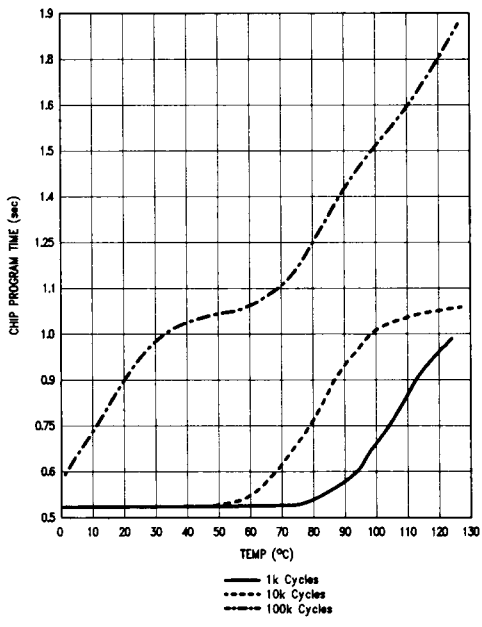


Figure 8. 28F256A Typical Program Time at 12V

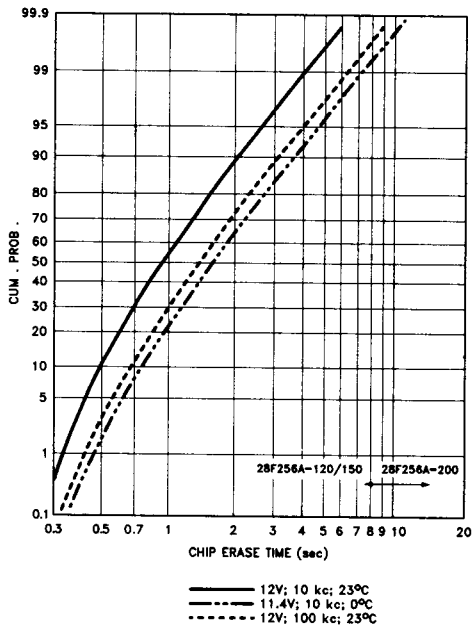


Figure 9. 28F256A Typical Erase Capability

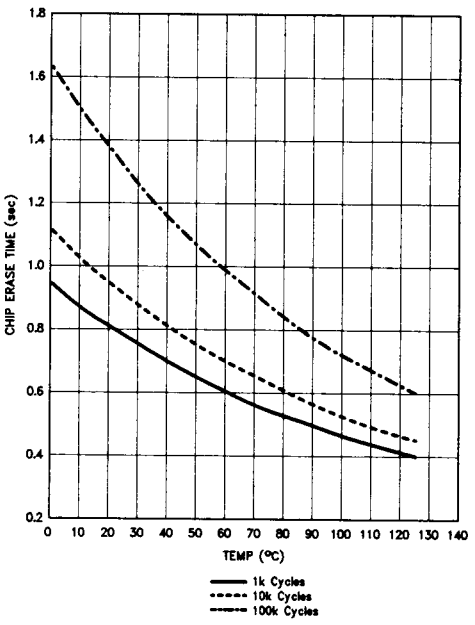


Figure 10. 28F256A Typical Erase Time at 12.0V

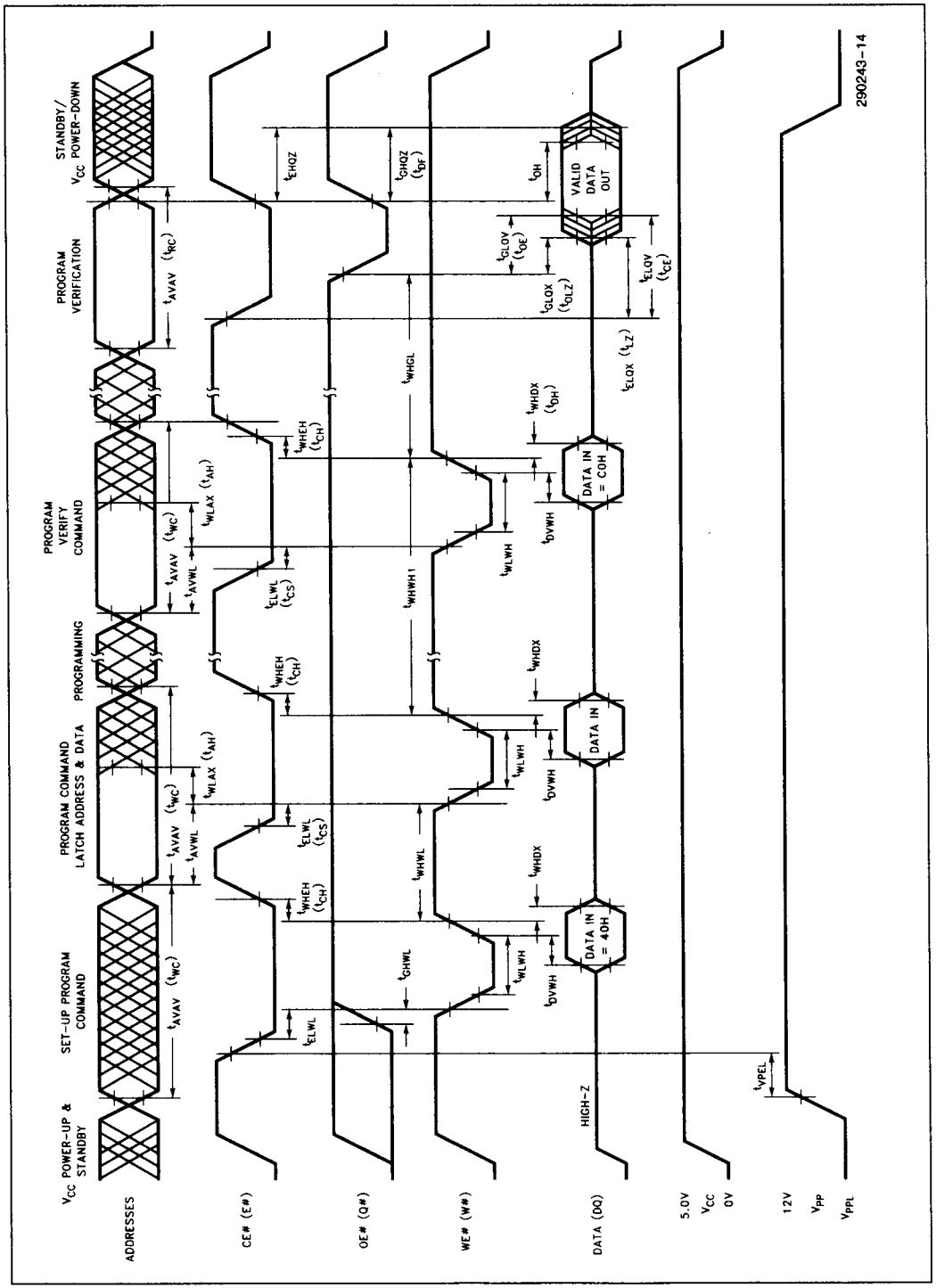


Figure 11. AC Waveforms for Programming Operations

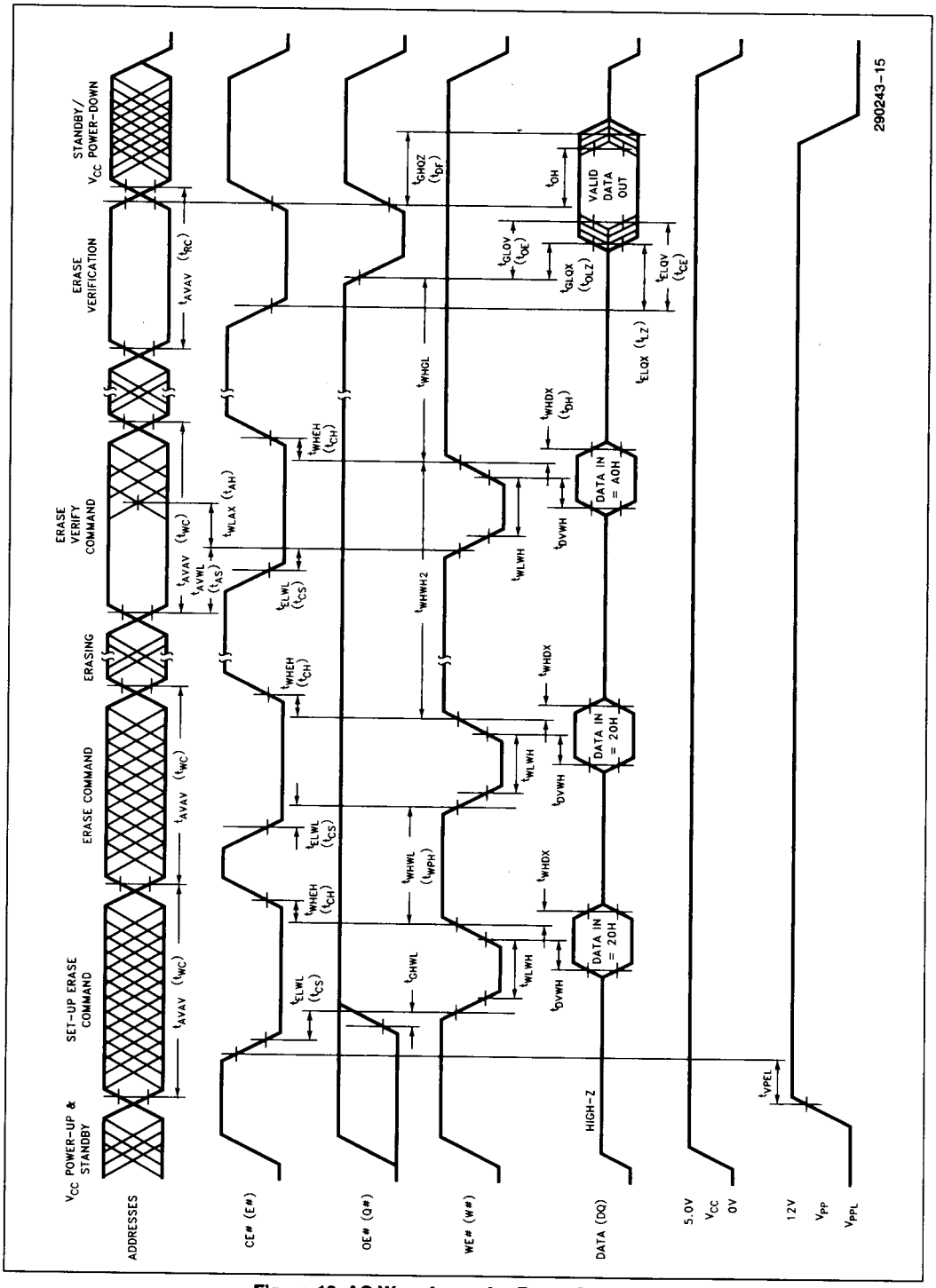


Figure 12. AC Waveforms for Erase Operations

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ALTERNATIVE CE#-CONTROLLED WRITES

Versions		Notes	28F256A-120		28F256A-150		Unit
Symbol	Characteristic		Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time		120		150		ns
t_{AVEL}	Address Set-Up Time		0		0		ns
t_{ELAX}	Address Hold Time		80		80		ns
t_{DVEH}	Data Set-Up Time		50		50		ns
t_{EHDX}	Data Hold Time		10		10		ns
t_{EHGL}	Write Recovery Time before Read		6		6		µs
t_{GHEL}	Read Recover Time before Write	2	0		0		µs
t_{WLEL}	Write Enable Set-Up Time before Chip-Enable		0		0		ns
t_{EHWH}	Write Enable Hold Time		0		0		ns
t_{ELEH}	Write Pulse Width	1	70		70		ns
t_{EHEL}	Write Pulse Width High		20		20		ns
t_{VPEL}	V_{PP} Set-Up Time to Chip-Enable Low	2	1.0		1.0		µs

NOTE:
1. Chip-Enable Controlled Writes: Write operations are driven by the valid combination of Chip-Enable and Write-Enable. In systems where Chip-Enable defines the write pulse width (with a longer Write-Enable timing waveform) all set-up, hold and inactive Write-Enable times should be measured relative to the Chip-Enable waveform.
2. Guaranteed by design.

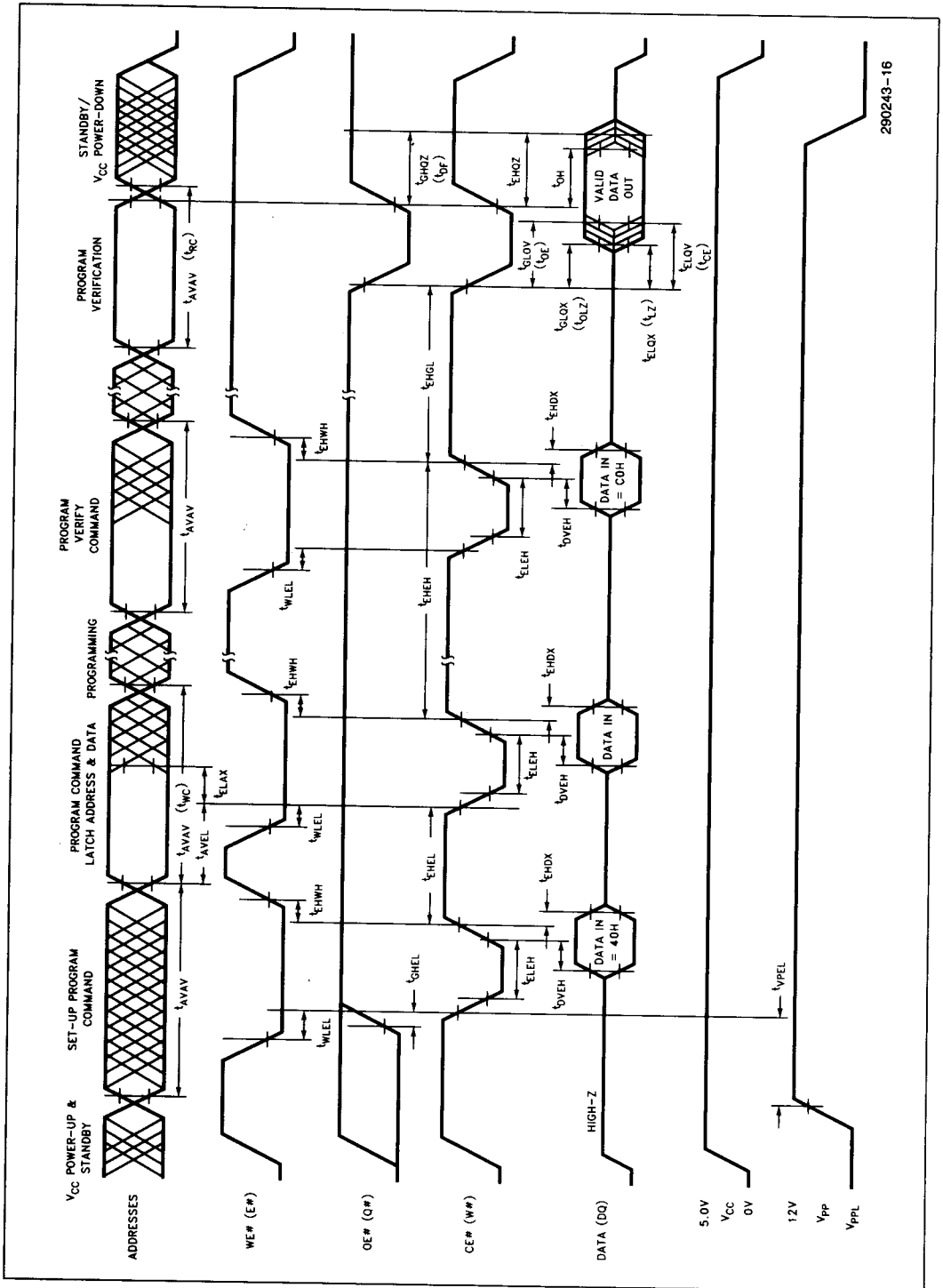

Figure 13. Alternate AC Waveforms for Programming Operations

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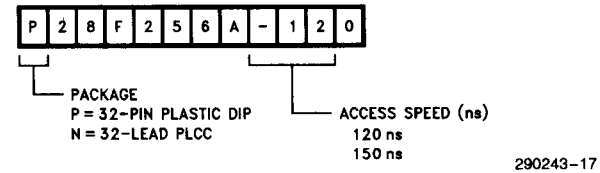
ORDERING INFORMATION



VALID COMBINATIONS:
P28F256A-120
P28F256A-150
N28F256A-120
N28F256A-150

ADDITIONAL INFORMATION

		Order Number
ER-20,	"ETOX II Flash Memory Technology"	294005
ER-24,	"Intel Flash Memory"	294008
RR-60,	"ETOX II Flash Memory Reliability Data Summary"	293002
AP-316,	"Using Flash Memory for In-System Reprogramming Nonvolatile Storage"	292046
AP-325,	"Guide to Flash Memory Reprogramming"	292059

REVISION HISTORY

Number	Description
004	Removed **Preliminary** Classification. Removed **200 ns** speed bin. Revised Erase Maximum Pulse Count for Figure 5 from **3000** to **1000**. Clarified AC and DC test conditions.
005	Corrected AC waveforms.
006	Revised symbols; i.e., $\overline{CE}$, $\overline{OE}$, etc. to CE#, OE#, etc.