Fast Page Mode (FPM) DRAM SIMM

322006-S51T04JD Pin 2Mx32 FPM SIMM
Unbuffered, 1k Refresh, 5V

General Description

The module is a 2Mx32 bit, 4 chip, 5V, 72 Pin SIMM module consisting of (4) 1Mx16 (SOJ) DRAM. The module is unbuffered and supports Fast Page Mode (FPM) access.

Pin Assignment

Pin #	Symbol	Pin #	Symbol	Pin #	Symbol	Pin #	Symbol
1	Vss	19	NC	37	DQ17	55	DQ12
2	DQ0	20	DQ4	38	DQ35	56	DQ30
3	DQ18	21	DQ22	39	Vss	57	DQ13
4	DQ1	22	DQ5	40	CAS0*	58	DQ31
5	DQ19	23	DQ23	41	CAS2*	59	Vcc
6	DQ2	24	DQ6	42	CAS3*	60	DQ32
7	DQ20	25	DQ24	43	CAS1*	61	DQ14
8	DQ3	26	DQ7	44	RAS0*	62	DQ33
9	DQ21	27	DQ25	45	RAS1*	63	DQ15
10	Vcc	28	A7	46	NC	64	DQ34
11	PD5	29	NC	47	WE*	65	DQ16
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PD1
14	A2	32	A9	50	DQ27	68	PD2
15	A3	33	RAS3*	51	DQ10	69	PD3
16	A4	34	RAS2*	52	DQ28	70	PD4
17	A5	35	DQ26	53	DQ11	71	NC
18	A6	36	DQ8	54	DQ29	72	Vss

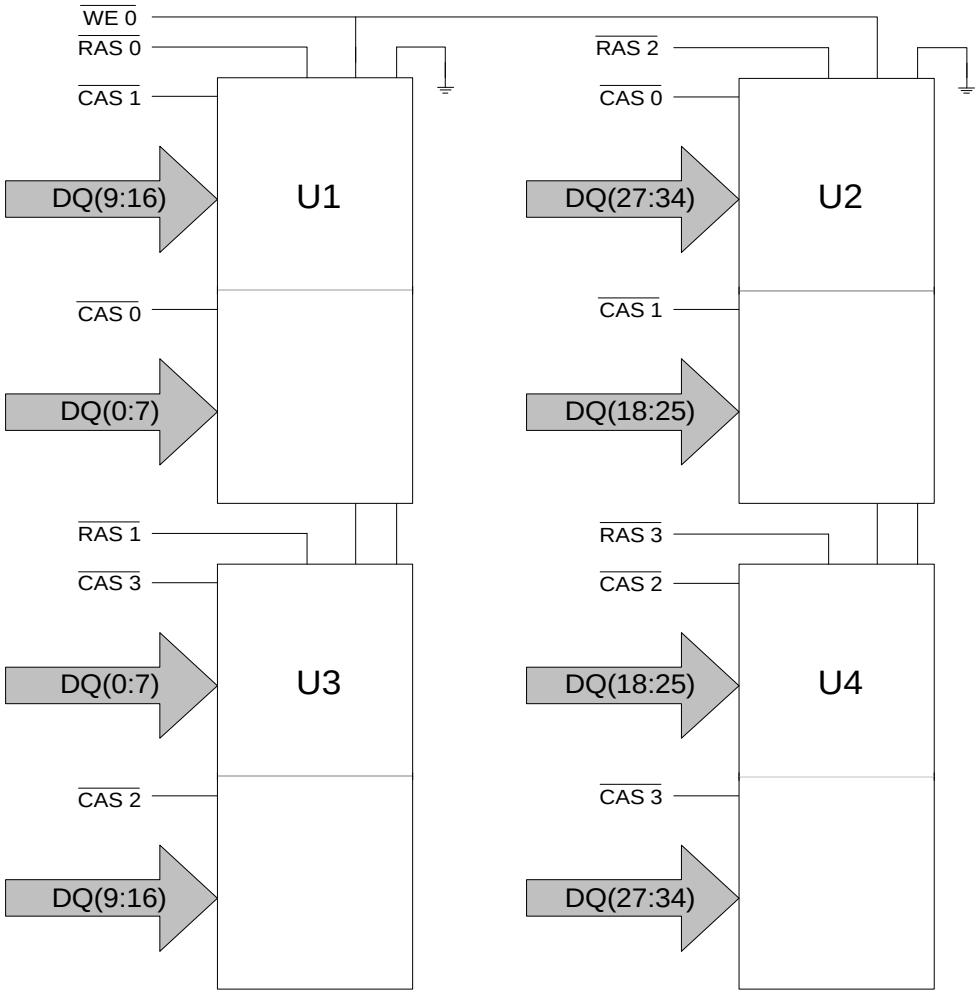
* Active Low

Features

- JEDEC-Standard 72-pin Single Inline Memory Module (SIMM)
- Unbuffered
- 60ns access time
- Supports Fast Page Mode (FPM) access cycles.
- Based on 1Mx16 DRAM
- Power Supply: 5.0V ± 0.5V
- 16ms, 1024-cycle refresh
- Supports RAS-Only-Refresh (ROR), CAS-before-RAS (CBR) refresh and Hidden refresh cycles
- Four Presence Detect (PD) lines
- TTL Compatible Inputs and Outputs
- Two External Banks
- Gold PCB connector

Block Diagram

X32 DRAM SIMM, 2 BANK with X16 DRAMs



A0 - AN → A0 - AN: DRAMs U1 - U4

O.22UF, 2 CAPS PER IC

VCC → U1 - U4

VSS → U1 - U4

PD: JUMPERS: J1 - J4

Pin Descriptions

Pin	Name	Function
RAS#	Row Address Strobe	RAS# is used to strobe row addresses.
CAS#	Column Address Strobe	CAS# is used to strobe column addresses
WE#	Write Enable	WE# is used to control read/write cycles.
A#	Address Lines	Address lines are multiplexed to specify the row and column address.
DQ0-DQ35	Data Lines	Data input/output lines.
Vdd	Power Supply	Power Supply 5.0V±0.5V
Vss	Ground	Ground
PD#	Presence Detect Lines	Presence detect lines are used to specify Module type. Lines are either grounded or NC in module (see Presence Detect Matrix).
NC	No Connection	Line is not connected in module.

Presence Detect Matrix

Module Type	PD1	PD2	PD3	PD4
322006-S51T04JD	NC	NC	NC	NC

Absolute Maximum Ratings

Parameter	Symbol	Value	Units
Voltage on any pin relative to Vss	V_{in}	-1.0 to 7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	Pt	4	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{st}	-55 to +125	°C

NOTE: Permanent damage may occur if absolute maximum ratings are exceeded.
Device should be operated within recommended operating conditions only.

DC Characteristics (T_A = 0 to 70C, Vcc = 5.0V ± 0.5V)

Parameter	Symbol	Min	Typ	Max	Units	Note
Supply voltage	Vss	0	0	0	V	
Supply voltage	Vcc	4.5	5.0	5.5	V	16
Input high voltage	Vih	2.4	-	Vcc+1.0	V	16
Input low voltage	Vil	-1.0	-	0.8	V	16
Output high voltage	Voh	2.4	-	-	V	
Output low voltage	Vol	-	-	0.4	V	

DC Current Consumption (T_A = 0 to 70C, Vcc = 5.0V ± 0.5V)

Parameter	Symbol	Test Condition	-60	Unit	Note
Standby Current (TTL)	I_{CC1}	(RAS# = CAS# = V_{IH})	8	mA	17
Standby Current (CMOS)	I_{CC2}	All inputs = Vcc - 0.2V	4	mA	17
Operating Current Random Read/Write	I_{CC3}	RAS#, CAS#, address cycling. $t_{RC} = t_{RC[MIN]}$	260	mA	17, 18
Operating Current Fast Page Mode	I_{CC4}	RAS# = V_{IL}, CAS#, Address cycling. $t_{PC} = t_{PC[MIN]}$	104	mA	17, 18
Operating Current EDO Page Mode	I_{CC5}	RAS# = V_{IL}, CAS#, Address cycling. $t_{PC} = t_{PC[MIN]}$	-	mA	17, 18
Refresh Current: RAS#-Only	I_{CC6}	RAS# cycling, CAS#=V_{IH}; $t_{RC} = t_{RC[MIN]}$	260	mA	17
Refresh Current: CAS# before RAS#	I_{CC7}	RAS#, CAS#, address cycling $t_{RC} = t_{RC[MIN]}$	260	mA	17

Capacitance (T_A = 0 to 70C, Vcc = 5.0V ± 0.5V, Vss = 0V)

Parameter	Symbol	Typ	Max	Units	Note
Input capacitance (Address)	C_{I1}	-	20	pF	
Input capacitance (WE#, OE#)	C_{I2}	-	28	pF	
Input/Output capacitance (Data)	$C_{I/O}$	-	14	pF	
Input capacitance (CAS#)	C_{I3}	-	14	pF	
Input capacitance (RAS#)	C_{14}	-	7	pF	

AC Characteristics (T_A = 0 to 70C, Vcc = 5.0V ± 0.5V, Vss = 0V)

Parameter	Symbol	-60		Units	Note
		Min	Max		
Access time from column address	t_{AA}		30	ns	3, 5, 14
Column address setup to CAS# precharge	t_{ACH}	15		ns	
Column address hold time (from RAS#)	t_{AR}	50		ns	
Column address setup time	t_{ASC}	0		ns	
Row address setup time	t_{ASR}	0		ns	
Access time from CAS#	t_{CAC}		17	ns	3, 4, 14
Column address hold time	t_{CAH}	10		ns	
CAS# pulse width	t_{CAS}	10	10 000	ns	
CAS# to output in Low-Z	t_{CLZ}	3		ns	
Data output hold after CAS# LOW	t_{COH}	3		ns	
CAS# precharge time	t_{CP}	10		ns	
Access time from CAS# precharge	t_{CPA}		35	ns	
CAS# to RAS# precharge time	t_{CRP}	5		ns	
CAS# hold time	t_{CSH}	50		ns	
WRITE command to CAS# lead time	t_{CWL}	10		ns	
Data-in hold time	t_{DH}	10		ns	11
Data-in setup time	t_{DS}	0		ns	11
Output buffer turn-off delay	t_{OFF}	0	15	ns	
EDO Page-mode read or write cycle time	t_{PC}	25		ns	
Access time from RAS#	t_{RAC}		60	ns	2, 3
RAS# to column address delay time	t_{RAD}	15	30	ns	9
Row-address hold time	t_{RAH}	10		ns	
RAS# pulse width	t_{RAS}, t_{RASP}	60	10 000	ns	
Random read/write cycle time	t_{RC}	104		ns	
RAS# to CAS# delay time	t_{RCD}	20	43	ns	8
Read command hold time	t_{RCH}	0		ns	
Read command setup time	t_{RCS}	0		ns	
Refresh Period (1024 cycles)	t_{REF}		16	ms	15
RAS# precharge time	t_{RP}	40		ns	
RAS# to CAS# precharge time	t_{RPC}	5		ns	
READ command hold time	t_{RRH}	0		ns	
RAS# hold time	t_{RSH}	17		ns	
WRITE command to RAS# lead time	t_{RWL}	15		ns	
Transition Time	t_{τ}	2	50	ns	7

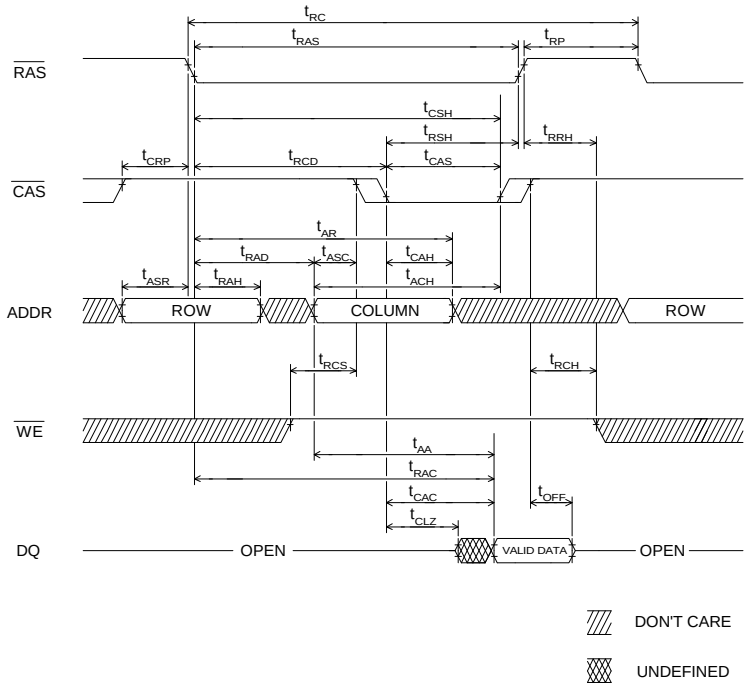
AC Characteristics (T_A = 0 to 70C, Vcc = 5.0V ± 0.5V, Vss = 0V)

Parameter	Symbol	-60		Units	Note
		Min	Max		
WRITE command hold time	t_{WCH}	10		ns	
WRITE command hold time (RAS# referenced)	t_{WCR}	45		ns	
WE# command setup time	t_{WCS}	0		ns	10
Output disable delay from WE#	t_{WHZ}	0	15	ns	
Write command pulse width	t_{WP}	5		ns	

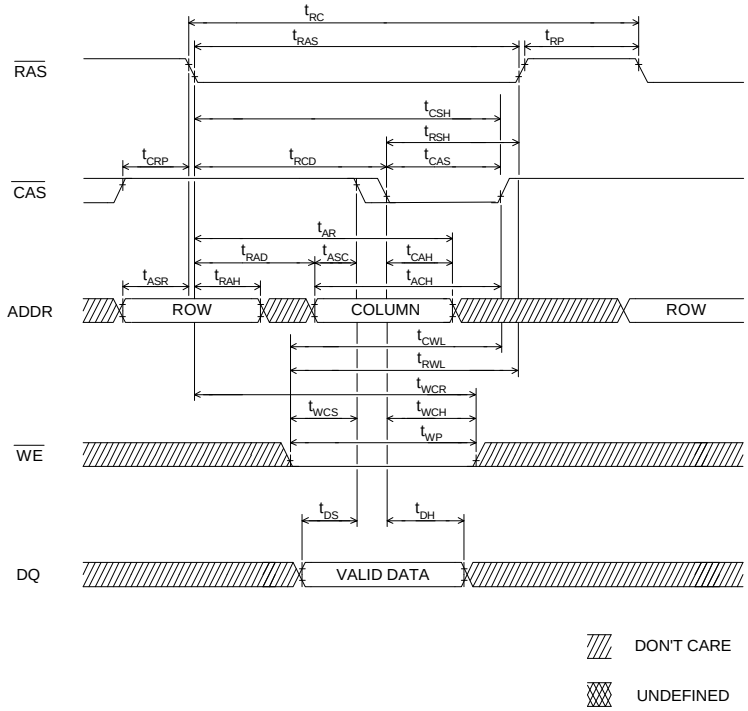
Notes

1. AC measurements assume t_T = 5ns
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max.) and $t_{RAD} \geq t_{RAD}$ (max.). If t_{RCD} or t_{RAD} is greater that the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivilaent to 1 TTL load and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max.), $t_{RAD} \leq t_{RAD}$ (max.).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max.), $t_{RAD} \geq t_{RAD}$ (max.).
6. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. Vih (min.) and Vil (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between Vih and Vil.
8. Operation with the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RCD} (max.) is specified as a reference point only, if t_{RCD} is greater that the specified t_{RCD} (max.) limit, then the access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RAD} (max.) is specified as a reference point only, if t_{RAD} is greater that the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min.))
11. These parameters are referenced to CAS* leading edge in an early write cycle.
12. An initial pause of 100us is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing RAS* clock such as RAS* only refresh)
13. t_{RASC} defines RAS* pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}
15. t_{REF} defined is 1,024 refresh cycle.
16. All voltages referenced to Vss
17. Typical maximum current consumption levels
18. Column address changed once per cycle

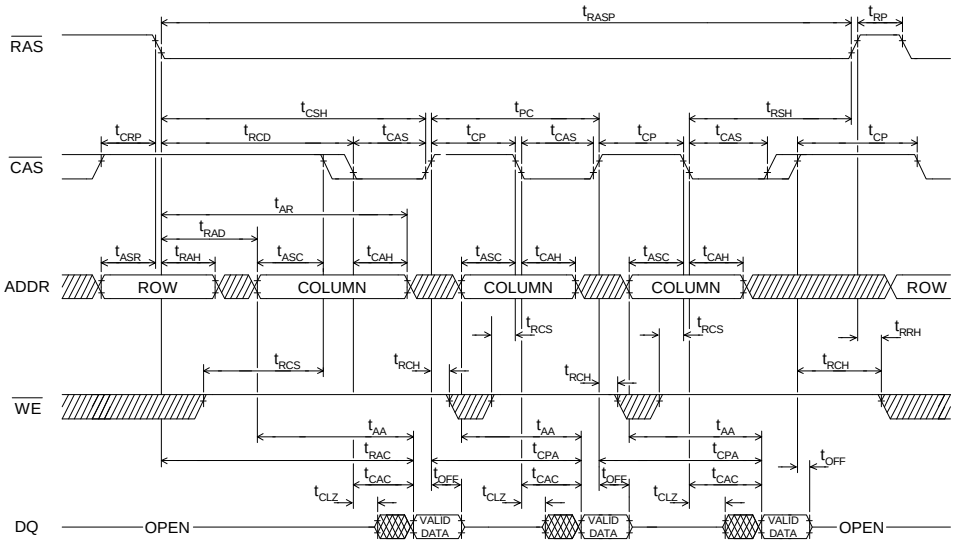
READ CYCLE



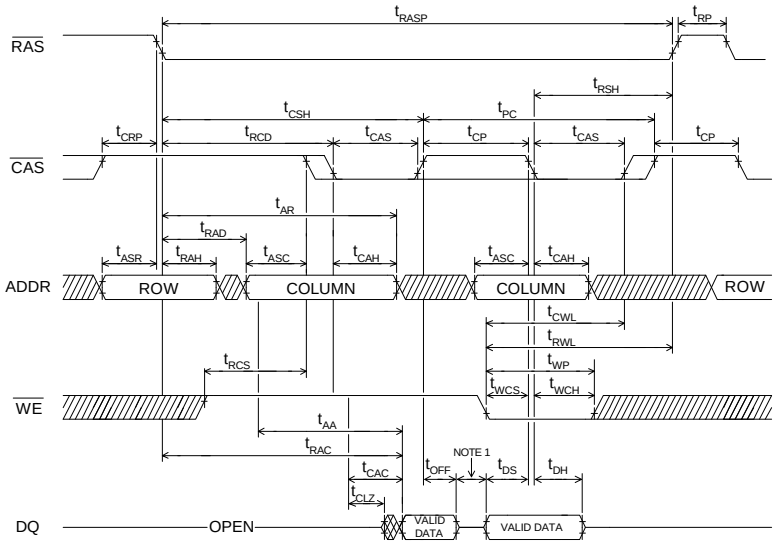
EARLY WRITE CYCLE



FAST-PAGE-MODE READ CYCLE

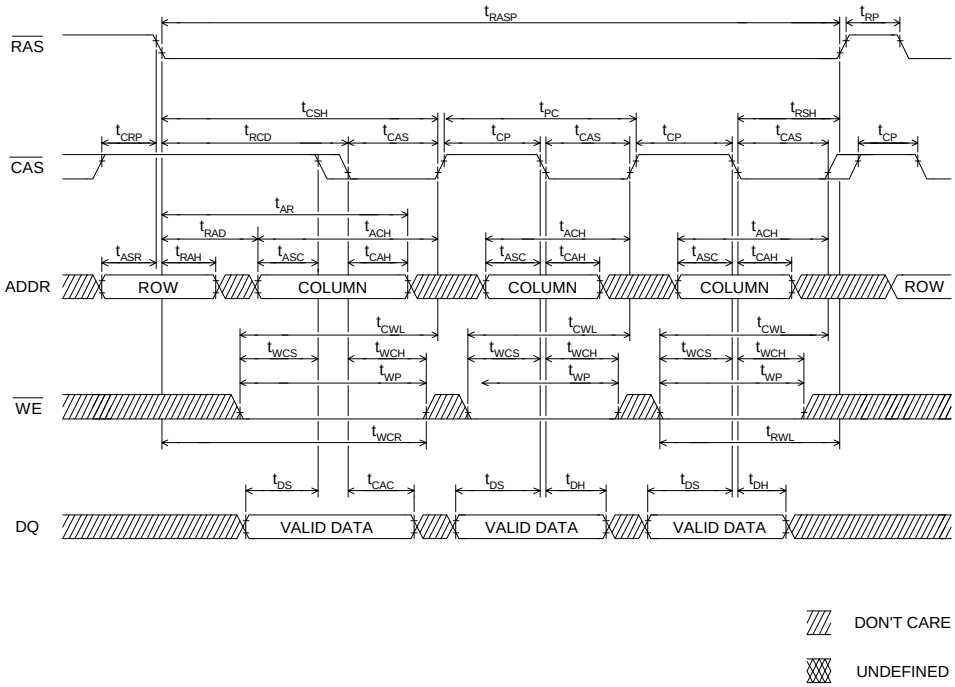


FAST-PAGE-MODE READ-EARLY-WRITE CYCLE

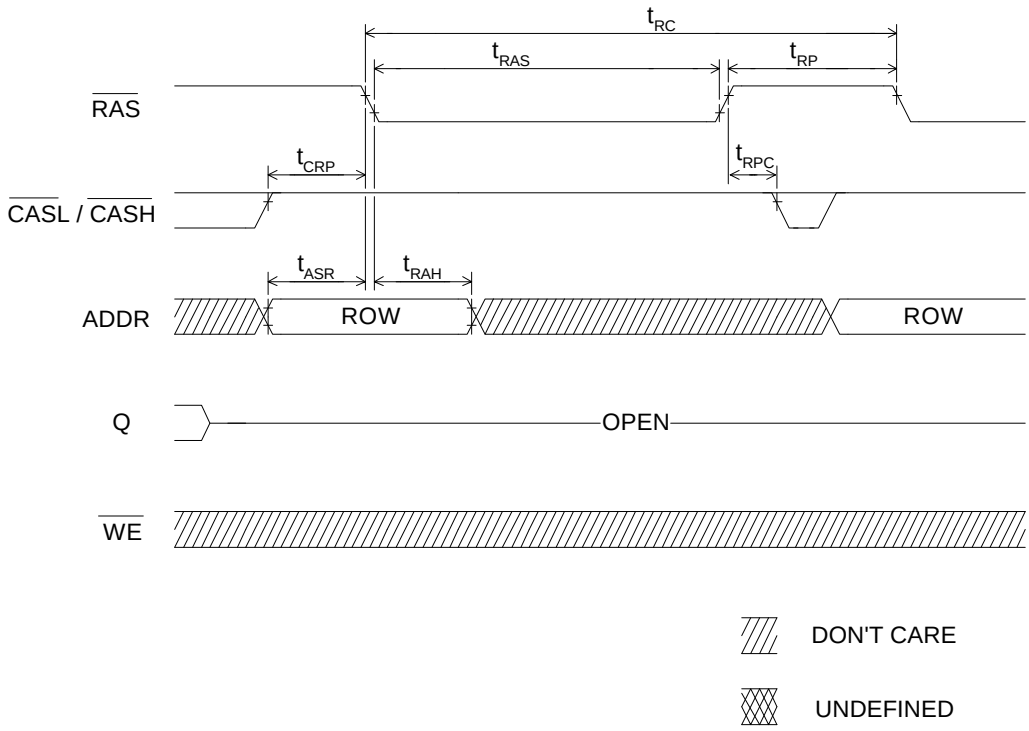


NOTE 1: DO NOT DRIVE DATA PRIOR TO TRISTATE

FAST/EDO-PAGE-MODE EARLY-WRITE CYCLE

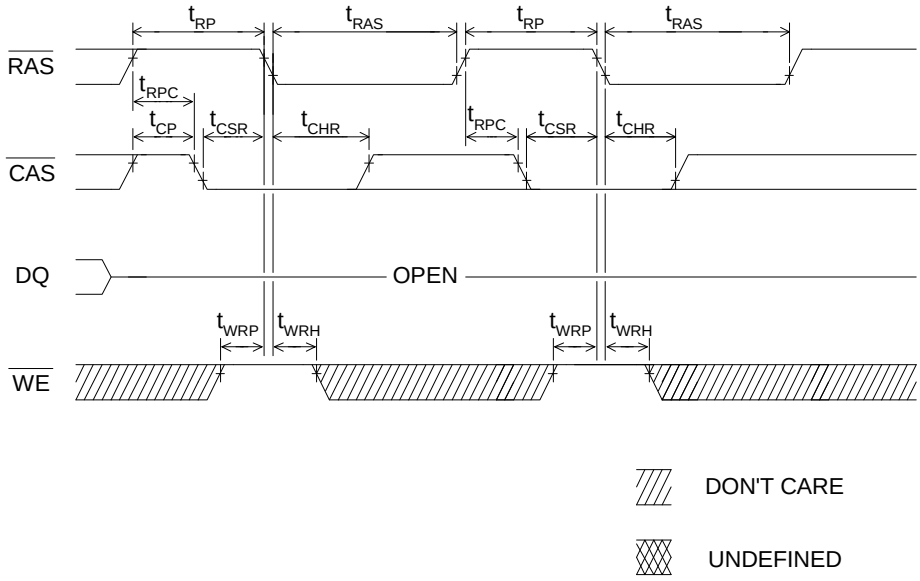


/RAS-ONLY REFRESH CYCLE

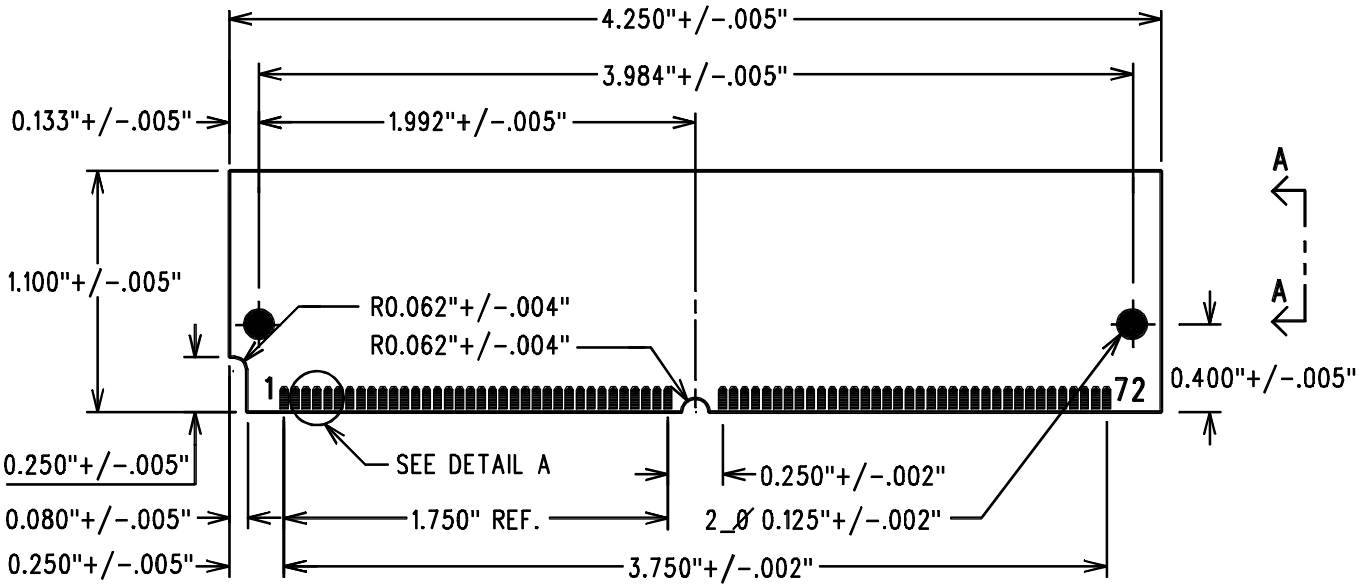


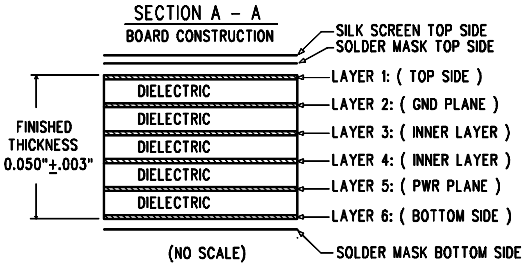
CBR REFRESH CYCLE

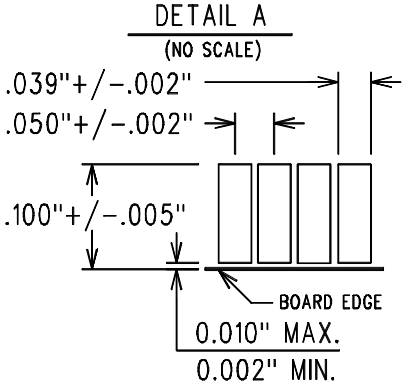
(Addresses = DON'T CARE)

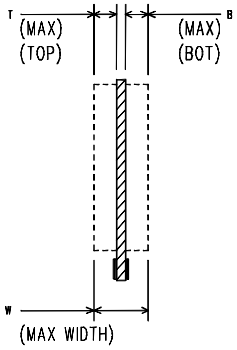


OUTLINE DRAWING



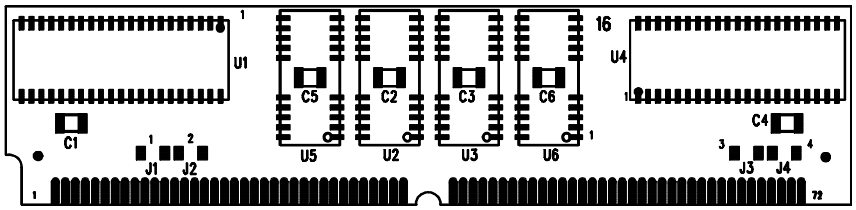






SIDEVIEW

FRONT VIEW



	W	T	B
SOJ	355	150	150

All units are in Mils

Note: Drawing is for component location only, assembly may not have all components installed.