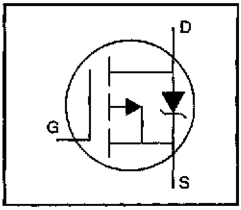
International
IOR Rectifier

PD-9.350F

IRF9610

HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- P-Channel
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements



$V_{DSS} = -200V$

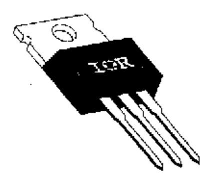
$R_{DS(on)} = 3.0\Omega$

$I_D = -1.8A$

Description

The HEXFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



TO-220AB

DATA SHEETS

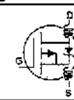
Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25°C$	Continuous Drain Current, V_{GS} @ -10 V	-1.8	A
I_D @ $T_C = 100°C$	Continuous Drain Current, V_{GS} @ -10 V	-1.0	
I_{DM}	Pulsed Drain Current ①	-7.0	
P_D @ $T_C = 25°C$	Power Dissipation	20	W
	Linear Derating Factor	0.16	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
I_{LM}	Inductive Current, Clamp	-7.0	A
dv/dt	Peak Diode Recovery dv/dt ③	-5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)	

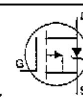
Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	6.4	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	

Electrical Characteristics @ $T_J = 25°C$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-200	—	—	V	V_{GS}=0V, I_D=-250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.23	—	V/°C	Reference to 25°C, I_D=-1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	3.0	Ω	V_{GS}=-10V, I_D=-0.90A ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	V_{DS}=V_{GS}, I_D=-250µA
g_{fs}	Forward Transconductance	0.90	—	—	S	V_{DS}=-50V, I_D=-0.90A ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	-100	µA	V_{DS}=-200V, V_{GS}=0V
		—	—	-500		V_{DS}=-160V, V_{GS}=0V, T_J=125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	V_{GS}=-20V
	Gate-to-Source Reverse Leakage	—	—	100		V_{GS}=20V
Q_g	Total Gate Charge	—	—	11	nC	I_D=-3.5A
Q_{gs}	Gate-to-Source Charge	—	—	7.0		V_{DS}=-160V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	4.0		V_{GS}=-10V See Fig. 11 & 18 ④
$t_{d(on)}$	Turn-On Delay Time	—	8.0	—	ns	V_{DD}=-100V
t_r	Rise Time	—	15	—		I_D=-0.90A
$t_{d(off)}$	Turn-Off Delay Time	—	10	—		R_G=50Ω
t_f	Fall Time	—	8.0	—		R_D=110Ω See Figure 17 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	170	—	pF	V_{GS}=0V
C_{oss}	Output Capacitance	—	50	—		V_{DS}=-25V
C_{rss}	Reverse Transfer Capacitance	—	15	—		f=1.0MHz See Figure 10

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-1.8	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-7.0		
V_{SD}	Diode Forward Voltage	—	—	-5.8	V	T_J=25°C, I_S=-1.8A, V_{GS}=0V ④
t_{rr}	Reverse Recovery Time	—	240	360	ns	T_J=25°C, I_F=-1.8A
Q_{rr}	Reverse Recovery Charge	—	1.7	2.6	µC	di/dt=100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is neglegible (turn-on is dominated by L_S-L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 5)

② Not Applicable

③ I_{SD}≤-1.8A, di/dt≤70A/µs, V_{DD}≤$V_{(BR)DSS}$, T_J≤150°C

④ Pulse width ≤ 300 µs; duty cycle ≤2%.

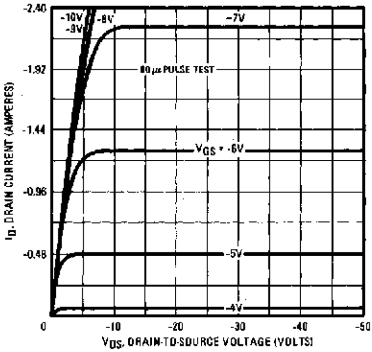


Fig. 1 — Typical Output Characteristics

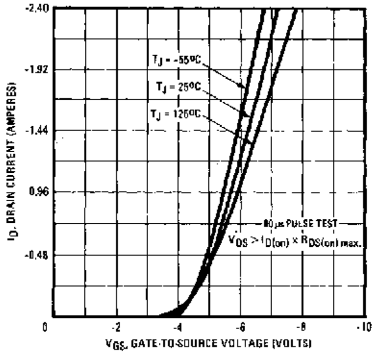


Fig. 2 — Typical Transfer Characteristics

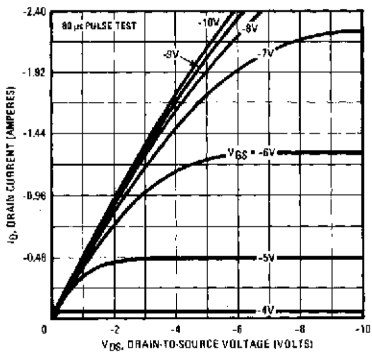


Fig. 3 — Typical Saturation Characteristics

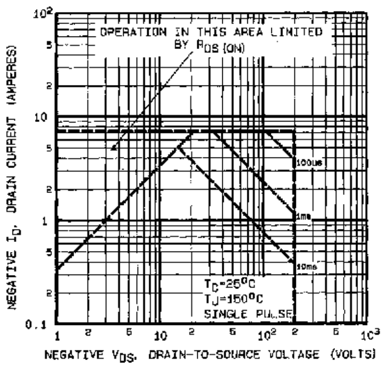


Fig. 4 — Maximum Safe Operating Area

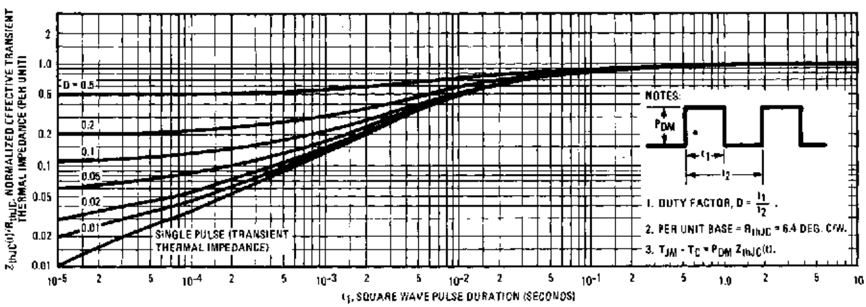


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

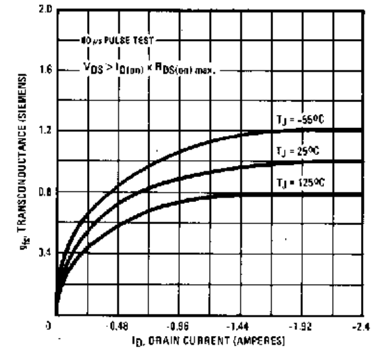


Fig. 6 — Typical Transconductance Vs. Drain Current

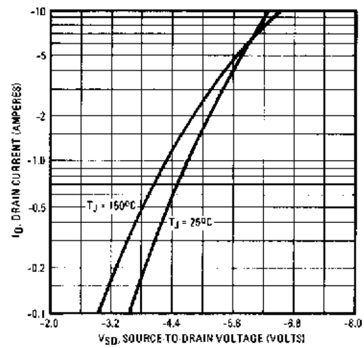


Fig. 7 — Typical Source-Drain Diode Forward Voltage

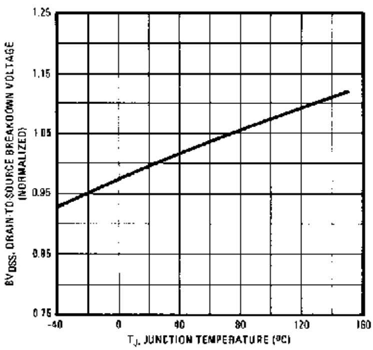


Fig. 8 — Breakdown Voltage Vs. Temperature

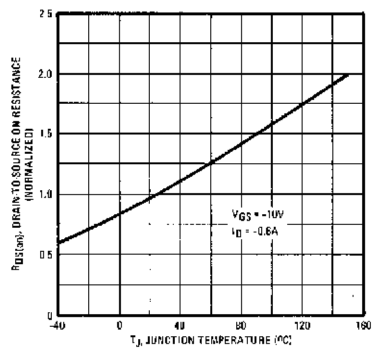


Fig. 9 — Normalized On-Resistance Vs. Temperature

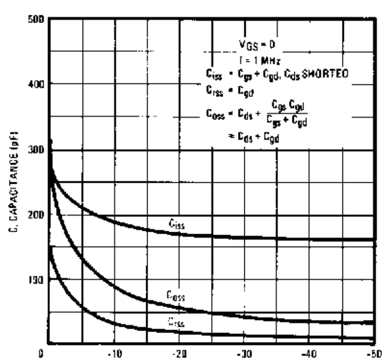


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

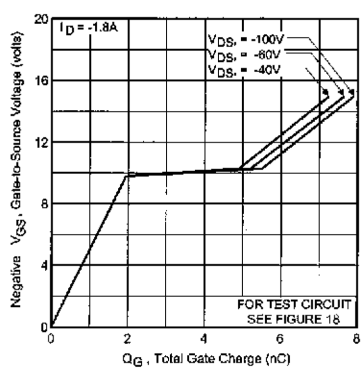


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

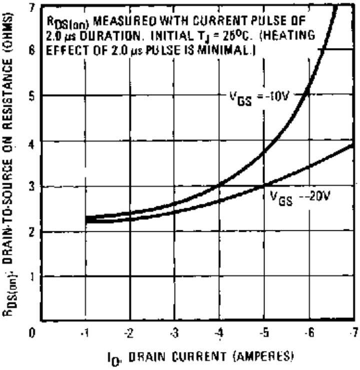


Fig. 12 — Typical On-Resistance Vs. Drain Current

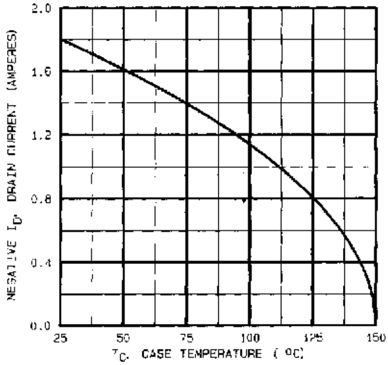


Fig. 13 — Maximum Drain Current Vs. Case Temperature

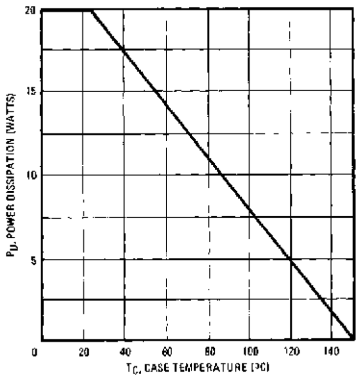


Fig. 14 — Power Vs. Temperature Derating Curve

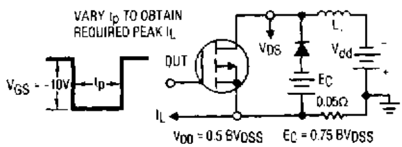


Fig. 15 — Clamped Inductive Test Circuit

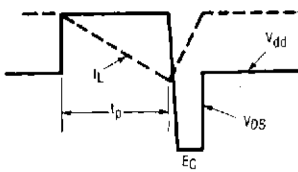


Fig. 16 — Clamped Inductive Waveforms

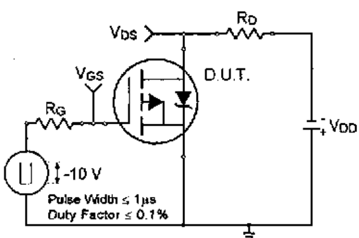


Fig. 17a — Switching Time Test Circuit

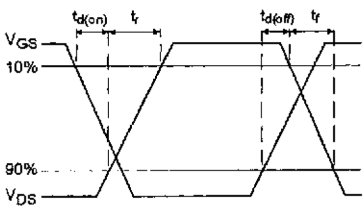


Fig. 17b — Switching Time Waveforms

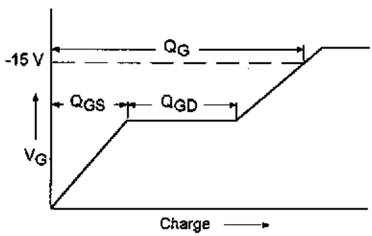


Fig. 18a — Basic Gate Charge Waveform

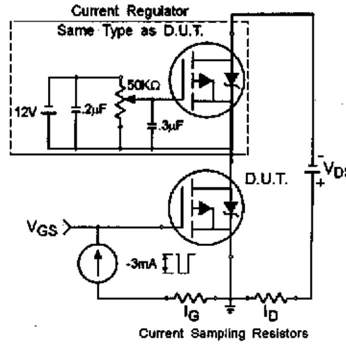


Fig. 18b — Gate Charge Test Circuit

Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit – See page 1506

Appendix B: Package Outline Mechanical Drawing – See page 1509

Appendix C: Part Marking Information – See page 1516

Appendix E: Optional Leadforms – See page 1525

International Rectifier

Notice

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