T-33-15
T-33-13

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MJ16010A
MJH16010A

POWER TRANSISTORS
15 AMPERES
500 VOLTS
125 and 175 WATTS

Designer's Data Sheet

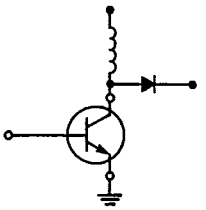
NPN Silicon Power Transistors

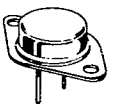
1 kV Switchmode III Series

These transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line-operated switchmode applications.

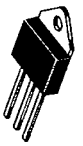
Typical Applications:
- Switching Regulators
- Inverters
- Solenoids
- Relay Drivers
- Motor Controls
- Deflection Circuits

Features:
- Collector-Emitter Voltage — V_{CEV} = 1000 Vdc
- Fast Turn-Off Times
  - 50 ns Inductive Fall Time – 100°C (Typ)
  - 90 ns Inductive Crossover Time – 100°C (Typ)
  - 900 ns Inductive Storage Time – 100°C (Typ)
- 100°C Performance Specified for:
  - Reverse-Biased SOA with Inductive Load
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents
- Extended FBSOA Rating Using Ultra-fast Rectifiers
- Extremely High RBSOA Capability





CASE 1-06
TO-204AA
MJ16010A



CASE 340-02
TO-218AC
MJH16010A

MAXIMUM RATINGS

Rating	Symbol	MJ16010A	MJH16010A	Unit
Collector-Emitter Voltage	V_{CEO}	500		Vdc
Collector-Emitter Voltage	V_{CEV}	1000		Vdc
Emitter-Base Voltage	V_{EB}	6		Vdc
Collector Current — Continuous — Peak(1)	I_C I_{CM}	15 20		Adc
Base Current — Continuous — Peak(1)	I_B I_{BM}	10 15		Adc
Total Power Dissipation @ T_C = 25°C @ T_C = 100°C Derate above T_C = 25°C	P_D	175 100 1	135 54 1.09	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to 200	−55 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max		Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	0.92	°C/W
Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275		°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS(1)					
Collector-Emitter Sustaining Voltage (Table 1) (I_C = 100 mA, I_B = 0)	$V_{CEO(sus)}$	500	—	—	Vdc
Collector Cutoff Current (V_{CEV} = 1000 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CEV} = 1000 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)	I_{CEV}	— —	0.003 0.020	0.15 1.0	mAdc
Collector Cutoff Current (V_{CE} = 1000 Vdc, R_{BE} = 50 Ω, T_C = 100°C)	I_{CER}	—	0.020	1.0	mAdc
Emitter Cutoff Current (V_{EB} = 6 Vdc, I_C = 0)	I_{EBO}	—	0.005	0.15	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$	See Figure 14a or 14b			
Clamped Inductive SOA with Base Reverse Biased	RBSOA	See Figure 15			
ON CHARACTERISTICS(1)					
Collector-Emitter Saturation Voltage (I_C = 5 Adc, I_B = 1 Adc) (I_C = 10 Adc, I_B = 2 Adc) (I_C = 10 Adc, I_B = 2 Adc, T_C = 100°C)	$V_{CE(sat)}$	— — —	0.25 0.45 0.60	0.7 1 1.5	Vdc
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2 Adc) (I_C = 10 Adc, I_B = 2 Adc, T_C = 100°C)	$V_{BE(sat)}$	— —	1.2 1.2	1.5 1.5	Vdc
DC Current Gain (I_C = 15 Adc, V_{CE} = 5 Vdc)	h_{FE}	5	8	—	—
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 kHz)	C_{ob}	—	—	400	pF

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SWITCHING CHARACTERISTICS

Inductive Load (Table 1)							
Storage Time	(I_C = 10 Adc, I_{B1} = 1.3 Adc, $V_{BE(off)}$ = 5 Vdc, $V_{CE(pk)}$ = 400 Vdc)	(T_J = 100°C)	t_{sv}	—	900	2000	ns
Fall Time			t_{fi}	—	50	250	
Crossover Time			t_c	—	90	300	
Storage Time		(T_J = 150°C)	t_{sv}	—	1100	—	
Fall Time			t_{fi}	—	70	—	
Crossover Time			t_c	—	120	—	
Resistive Load (Table 2)							
Delay Time	(I_C = 10 Adc, V_{CC} = 250 Vdc, I_{B1} = 1.3 Adc, PW = 30 μs, Duty Cycle ≤ 2%)	(I_{B2} = 2.6 Adc, R_{B2} = 1.6 Ω)	t_d	—	25	100	ns
Rise Time			t_r	—	325	600	
Storage Time			t_s	—	1300	3000	
Fall Time			t_f	—	175	400	
Storage Time		($V_{BE(off)}$ = 5 Vdc)	t_s	—	700	—	
Fall Time			t_f	—	80	—	

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

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TYPICAL STATIC CHARACTERISTICS

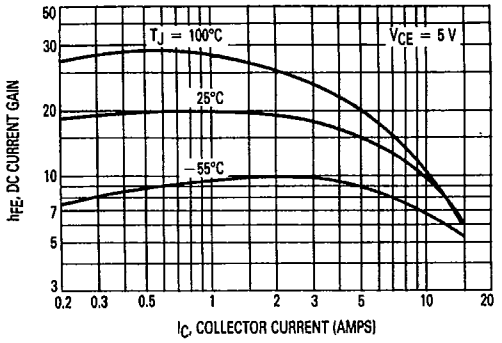

Figure 1. DC Current Gain

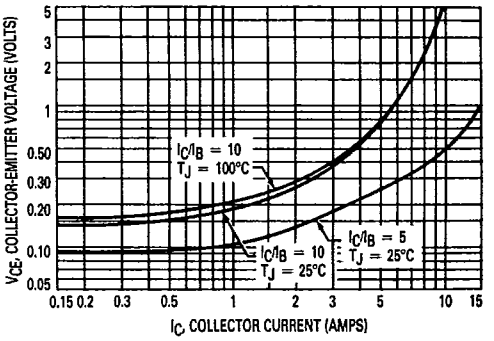

Figure 2. Collector-Emitter Saturation Region

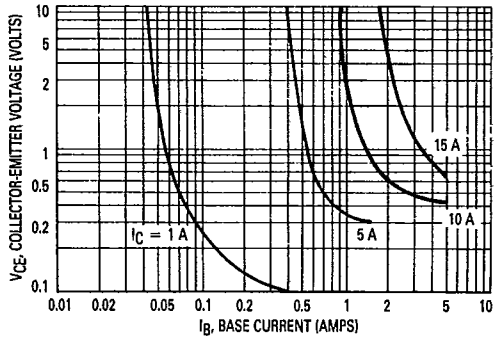

Figure 3. Collector-Emitter Saturation Region

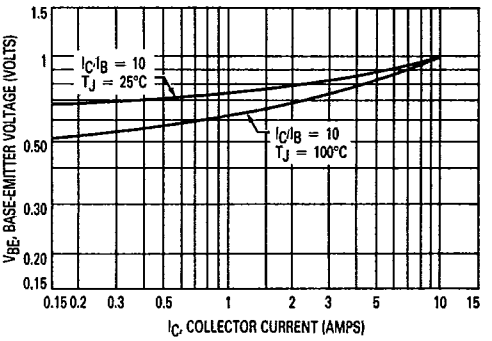

Figure 4. Base-Emitter Saturation Region

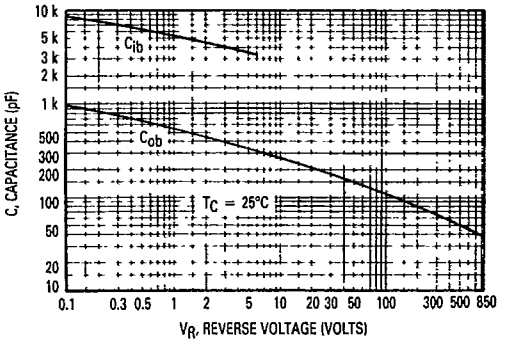

Figure 5. Capacitance

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TYPICAL INDUCTIVE SWITCHING CHARACTERISTICS

I_C/I_{B1} = 5, T_C = 75°C, $V_{CE(pk)}$ = 400 V

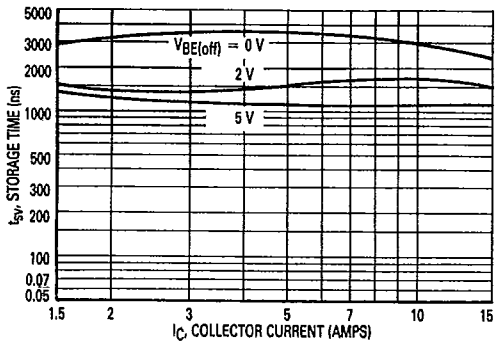

Figure 6. Storage Time

I_C/I_{B1} = 10, T_C = 75°C, $V_{CE(pk)}$ = 400 V

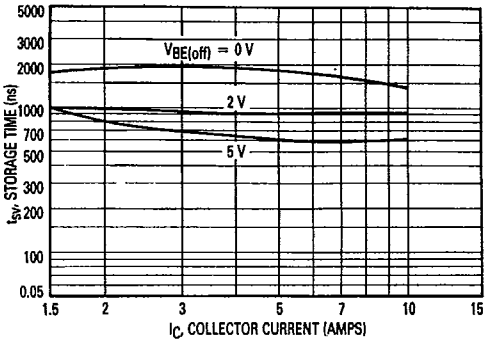

Figure 7. Storage Time

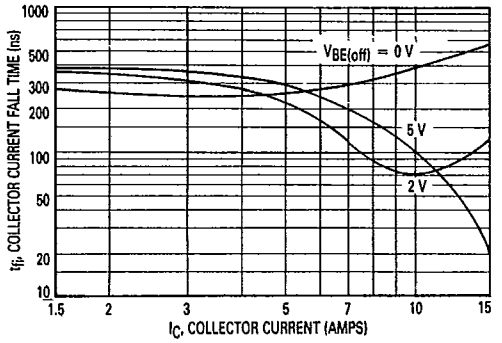

Figure 8. Collector Current Fall Time

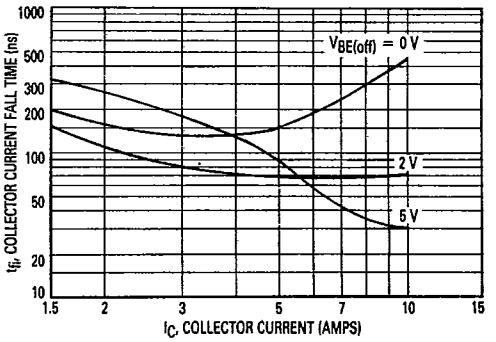

Figure 9. Collector Current Fall Time

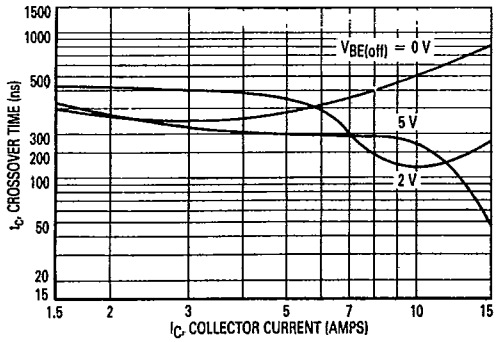

Figure 10. Crossover Time

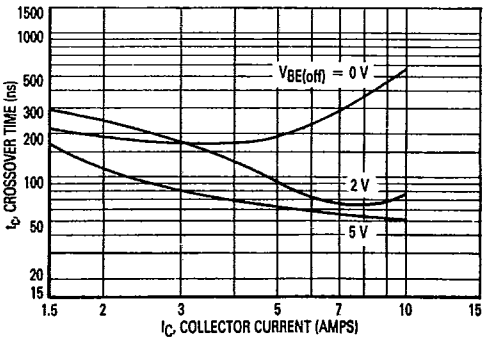

Figure 11. Crossover Time

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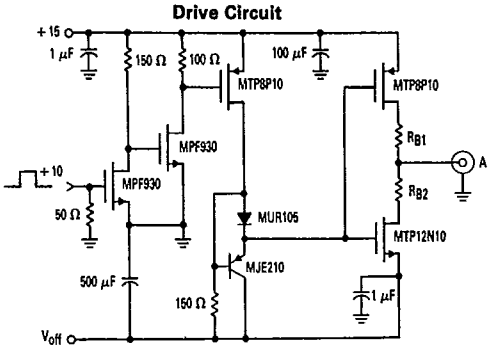
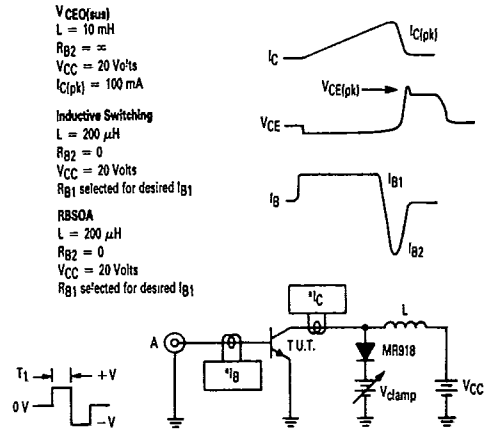
Table 1. Inductive Load Switching





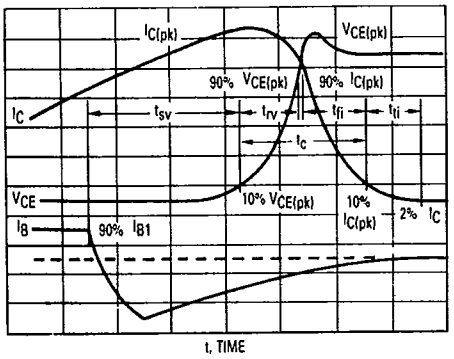


Figure 12. Inductive Switching Measurements

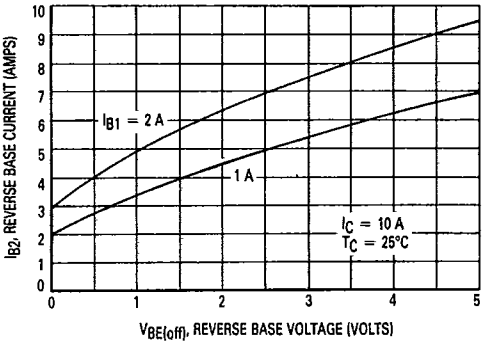
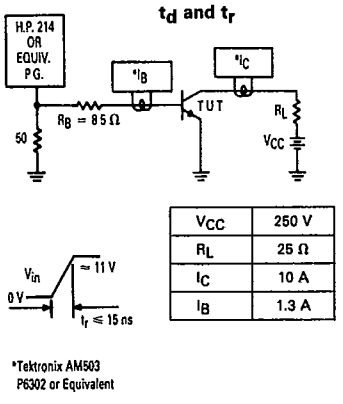
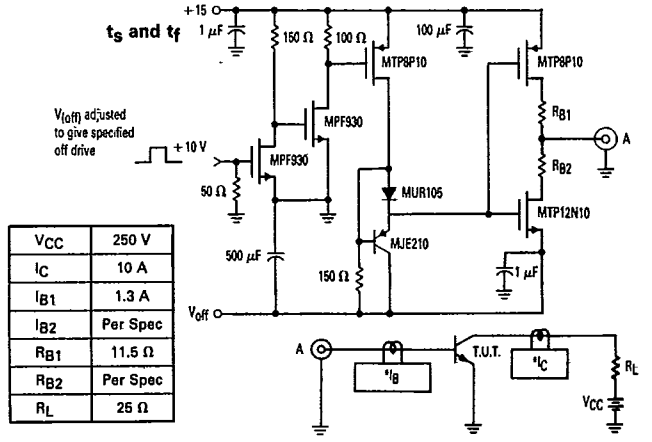


Figure 13. Peak Reverse Base Current

Table 2. Resistive Load Switching



V_{CC}	250 V
R_L	25 Ω
I_C	10 A
I_B	1.3 A



V_{CC}	250 V
I_C	10 A
I_{B1}	1.3 A
I_{B2}	Per Spec
R_{B1}	11.5 Ω
R_{B2}	Per Spec
R_L	25 Ω

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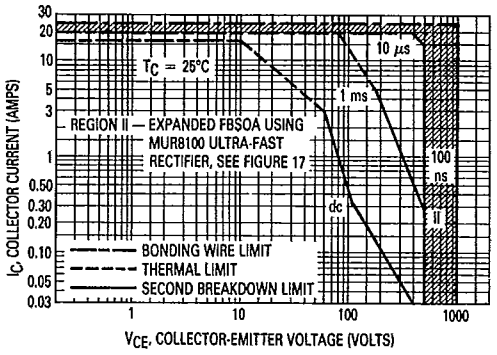
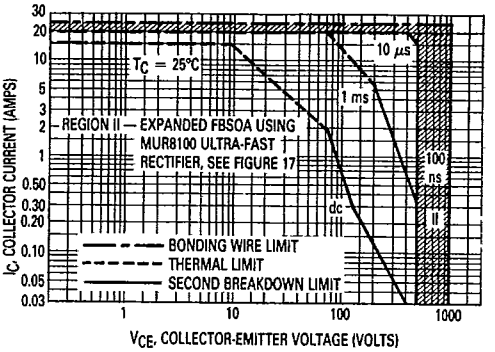
GUARANTEED OPERATING AREA INFORMATION



a. MJ16010A



b. MJH16010A

Figure 14. Maximum Rated Forward Biased Safe Operating Area

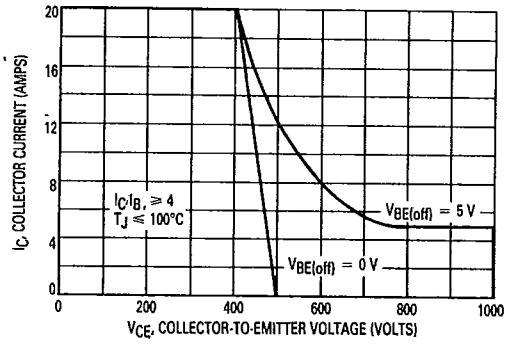


Figure 15. Maximum Reverse Biased Safe Operating Area

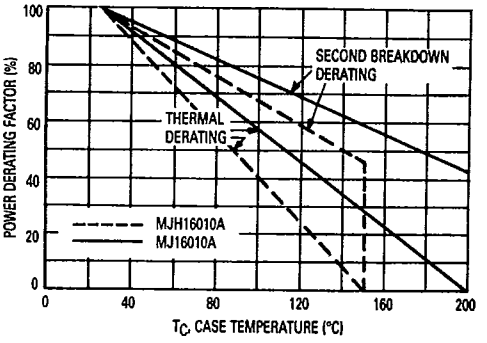


Figure 16. Power Derating

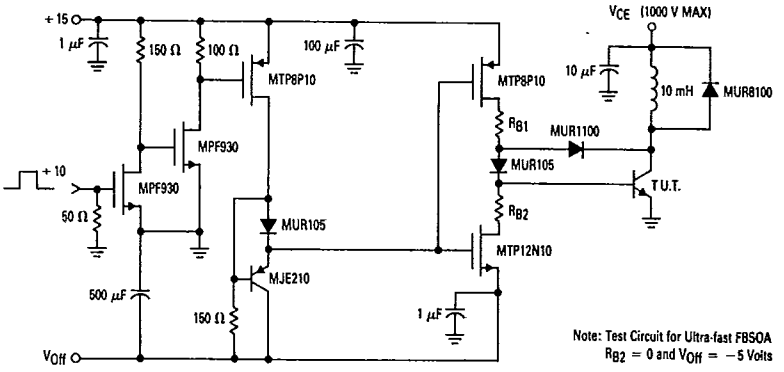


Figure 17. Switching Safe Operating Area

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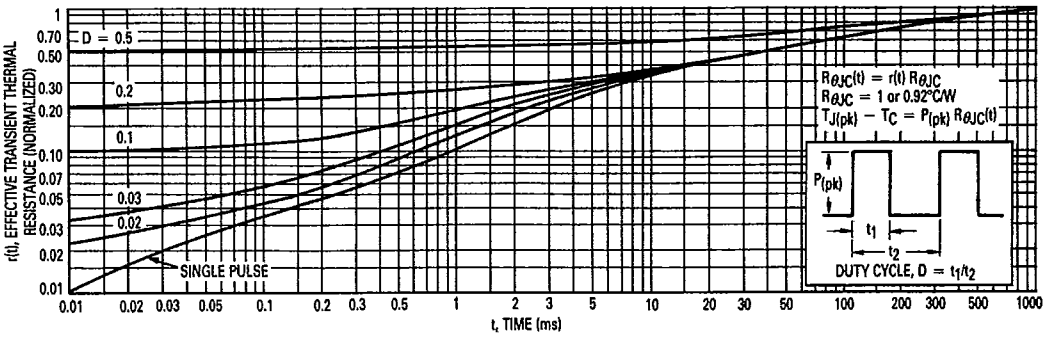

Figure 18. Thermal Response

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C—V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 14a and 14b is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figures 14a and 14b may be found at any case temperature by using the appropriate curve on Figure 16.

$T_{J(pk)}$ may be calculated from the data in Figure 18. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base-to-emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Biased Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 15 gives the RBSOA characteristics.

SWITCHMODE III DESIGN CONSIDERATIONS

1. FBSOA —

Allowable dc power dissipation in bipolar power transistors decreases dramatically with increasing collector-emitter voltage. A transistor which safely dissipates 100 watts at 10 volts will typically dissipate less than 10 watts at its rated $V_{CEO(sus)}$. From a power handling point of view, current and voltage are not interchangeable (see Application Note AN875).

2. TURN-ON —

Safe turn-on load line excursions are bounded by pulsed FBSOA curves. The 10 μs curve applies for resistive loads, most capacitive loads, and inductive loads that are clamped by standard or fast recovery rectifiers. Similarly, the 100 ns curve applies to inductive loads which are clamped by ultra-fast recovery rectifiers, and are valid for turn-on crossover times less than 100 ns (see Application Note AN952).

At voltages above 75% of $V_{CEO(sus)}$, it is essential to provide the transistor with an adequate amount of base drive VERY RAPIDLY at turn-on. More specifically, safe operation according to the curves is dependent upon base current rise time being less than collector current rise time. As a general rule, a base drive compliance voltage in excess of 10 volts is required to meet this condition (see Application Note AN875).

3. TURN-OFF —

A bipolar transistor's ability to withstand turn-off stress is dependent upon its forward base drive. Gross overdrive violates the RBSOA curve and risks transistor failure. For this reason, circuits which use fixed base drive are often more likely to fail at light loads due to heavy overdrive (see Application Note AN875).

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SWITCHMODE III DESIGN CONSIDERATIONS (Cont.)

4. OPERATION ABOVE $V_{CEO(sus)}$ —

When bipolars are operated above collector-emitter breakdown, base drive is crucial. A rapid application of adequate forward base current is needed for safe turn-on, as is a stiff negative bias needed for safe turn-off. Any hiccup in the base-drive circuitry that even momentarily violates either of these conditions will likely cause the transistor to fail. Therefore, it is important to design the driver so that its output is negative in the absence of anything but a clean crisp input signal (see Application Note AN952).

5. RBSOA —

Reverse Biased Safe Operating Area has a first order dependency on circuit configuration and drive parameters. The RBSOA curves in this data sheet are valid only for the conditions specified. For a comparison of RBSOA results in several types of circuits (see Application Note AN951).

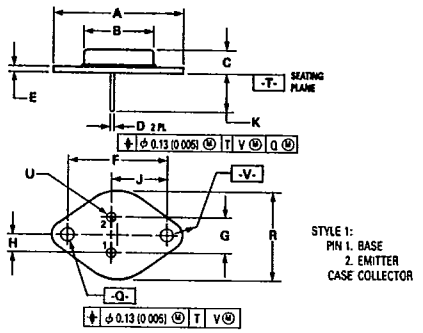
6. DESIGN SAMPLES —

Transistor parameters tend to vary much more from wafer lot to wafer lot, over long periods of time, than from one device to the next in the same wafer lot. For design evaluation it is advisable to use transistors from several different date codes.

7. BAKER CLAMPS —

Many unanticipated pitfalls can be avoided by using Baker Clamps. MUR105 and MUR1100 diodes are recommended for base drives less than 1 amp. Similarly, MUR405 and MUR4100 types are well-suited for higher drive requirements (see Article Reprint AR131).

OUTLINE DIMENSIONS

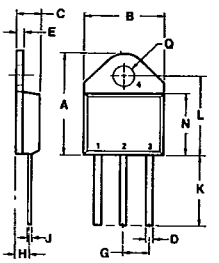


STYLE 1:
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES.
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2. CONTROLLING DIMENSION, INCH
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

CASE 1-06
TO-204AA
MJ16010A



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.41	3.20	0.095	0.126
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

CASE 340-02
TO-218AC
MJH16010A

3