Data Sheet
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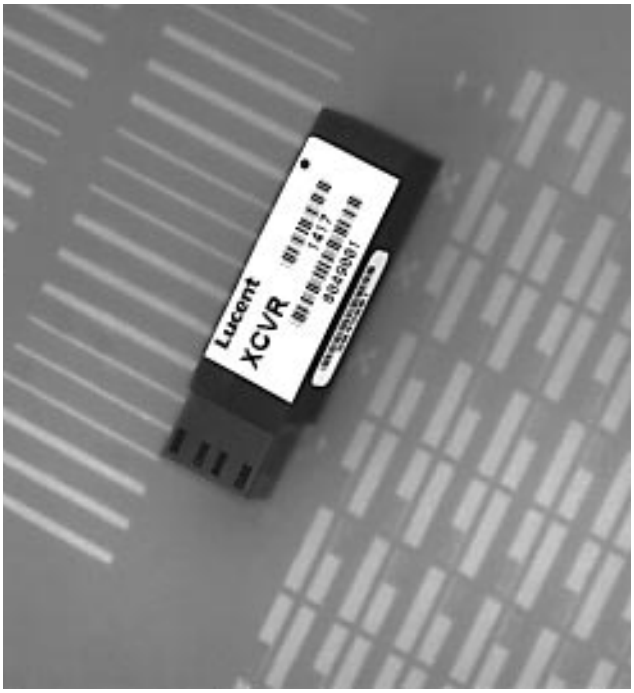
microelectronics group

Lucent Technologies
Bell Labs Innovations

# *NetLight*™ 1417G5 and 1417H5-Type ATM/SONET/SDH Transceivers with Clock Recovery




**Available in a small form factor, RJ-45 size, plastic package, the 1417G5 and 1417H5-Type are high-performance, cost-effective transceivers for ATM/SONET/SDH applications at 155 Mbits/s and 622 Mbits/s.**

## Features

- SONET/SDH Compliant (ITU-T G.957 Specifications)
  — IR-1/S1.1, S4.1
- Small form factor, RJ-45 size, multisourced 20-pin package
- Requires single 3.3 V power supply
- Clock recovery
- LC duplex receptacle
- Analog alarm outputs
- Uncooled 1300 nm laser transmitter with automatic output power control
- Transmitter disable input
- Wide dynamic range receiver with InGaAs PIN photodetector
- LVTTL signal-detect output
- Low power dissipation
- Raised ECL (PECL) logic data and clock interfaces
- Operating case temperature range: –40 °C to +85 °C
- Lucent Reliability and Qualification Program for built-in quality and reliability

## Description

The 1417G5 and 1417H5 transceivers are high-speed, cost-effective optical transceivers that are compliant with the International Telecommunication Union Telecommunication (ITU-T) G.957 specifications for use in ATM, SONET, and SDH applications. The 1417G5 operates at the OC-3/STM-1 rate of 155 Mbits/s, and the 1417H5 operates at the OC-12/STM-4 rate of 622 Mbits/s. The transceiver features Lucent's high-reliability optics and is packaged in a narrow-width plastic housing with an LC duplex receptacle. This receptacle fits into an RJ-45 form factor outline. The 20-pin package and pinout conform to a multisource transceiver agreement.

The transmitter features differential PECL logic level data inputs and a LVTTL logic level disable input. The receiver features differential PECL logic level data and clock outputs and a LVTTL logic level signal-detect output.

## Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 0 | 3.6 | V |
| Operating Case Temperature Range | $T_C$ | –40 | 85 | °C |
| Storage Case Temperature Range | $T_{stg}$ | –40 | 85 | °C |
| Lead Soldering Temperature/Time | — | — | 250/10 | °C/s |
| Operating Wavelength Range | λ | 1.1 | 1.6 | nm |

## Pin Information

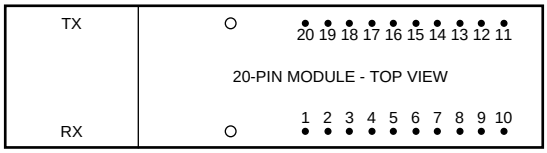



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**Figure 1. 1417G5 and 1714H5 Transceivers, 20-Pin Configuration, Top View**

**Table 1. Transceiver Pin Descriptions**

| Pin Number | Symbol | Name/Description | Logic Family |
|---|---|---|---|
| | | **Receiver** | |
| MS | MS | **Mounting Studs.** The mounting studs are provided for transceiver mechanical attachment to the circuit board. They may also provide an optional connection of the transceiver to the equipment chassis ground. | NA |
| 1 | Photodetector Bias | **Photodetector Bias.** This lead supplies bias for the PIN photodetector diode. | NA |
| 2 | $V_{EER}$ | **Receiver Signal Ground.** | NA |
| 3 | $V_{EER}$ | **Receiver Signal Ground.** | NA |
| 4 | CLK– | **Received Recovered $\overline{\text{Clock}}$ Out.** The rising edge occurs at the rising edge of the received data output. The falling edge occurs in the middle of the received data bit period. | PECL |
| 5 | CLK+ | **Received Recovered Clock Out.** The falling edge occurs at the rising edge of the received data output. The rising edge occurs in the middle of the received data bit period. | PECL |
| 6 | $V_{EER}$ | **Receiver Signal Ground.** | NA |
| 7 | $V_{CCR}$ | **Receiver Power Supply.** | NA |
| 8 | SD | **Signal Detect.**<br>Normal operation: logic one output.<br>Fault condition: logic zero output. | LVTTL |
| 9 | RD– | **Received $\overline{\text{DATA}}$ Out.** No internal terminations will be provided. | PECL |

## Pin Information (continued)

**Table 1. Transceiver Pin Descriptions** (continued)

| Pin Number | Symbol | Name/Description | Logic Family |
|---|---|---|---|
| 10 | RD+ | **Received DATA Out.** No internal terminations will be provided. | PECL |
| | | **Transmitter** | |
| 11 | $V_{CCT}$ | **Transmitter Power Supply.** | NA |
| 12 | $V_{EET}$ | **Transmitter Signal Ground.** | NA |
| 13 | $T_{DIS}$ | **Transmitter Disable.** | LVTTL |
| 14 | TD+ | **Transmitter Data In**. | PECL |
| 15 | TD– | **Transmitter Data In Bar**. | PECL |
| 16 | $V_{EET}$ | **Transmitter Signal Ground.** | NA |
| 17 | $B_{MON}$(–) | **Laser Diode Bias Current Monitor—Negative End.** The laser bias current is accessible as a dc-voltage by measuring the voltage developed across pins 17 and 18. | NA |
| 18 | $B_{MON}$(+) | **Laser Diode Bias Current Monitor—Positive End.** See pin 17 desciption. | NA |
| 19 | $P_{MON}$(–) | **Laser Diode Optical Power Monitor—Negative End.** The back-facet diode monitor current is accessible as a dc-voltage by measuring the voltage developed across pins 19 and 20. | NA |
| 20 | $P_{MON}$(+) | **Laser Diode Optical Power Monitor—Positive End.** See pin 19 desciption. | NA |

## Electrostatic Discharge

**Caution: This device is susceptible to damage as a result of electrostatic discharge (ESD). Take proper precautions during both handling and testing. Follow EIA standard EIA-625.**

Although protection circuitry is designed into the device, take proper precautions to avoid exposure to ESD. Lucent employs a human-body model (HBM) for ESD-susceptibility testing and protection-design evaluation. ESD voltage thresholds are dependent on the critical parameters used to define the model. A standard HBM (resistance = 1.5 kΩ, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes. The HBM ESD threshold established for the 1417G5 and 1417H5 transceivers is ±1000V.

## Application Information

The 1417 receiver section is a highly sensitive fiber-optic receiver. Although the data outputs are digital logic levels (PECL), the device should be thought of as an analog component. When laying out system application boards, the 1417 transceiver should receive the same type of consideration one would give to a sensitive analog component.

## Printed-Wiring Board Layout Considerations

A fiber-optic receiver employs a very high-gain, wide-bandwidth transimpedance amplifier. This amplifier detects and amplifies signals that are only tens of nA in amplitude when the receiver is operating near its sensitivity limit. Any unwanted signal currents that couple into the receiver circuitry cause a decrease in the receiver's sensitivity and can also degrade the performance of the receiver's signal detect (SD) circuit. To minimize the coupling of unwanted noise into the receiver, careful attention must be given to the printed-wiring board.

At a minimum, a double-sided printed-wiring board (PWB) with a large component-side ground plane beneath the transceiver must be used. In applications that include many other high-speed devices, a multilayer PWB is highly recommended. This permits the placement of power and ground on separate layers, which allows them to be isolated from the signal lines.

Multilayer construction also permits the routing of sensitive signal traces away from high-level, high-speed signal lines. To minimize the possibility of coupling noise into the receiver section, high-level, high-speed signals such as transmitter inputs and clock lines should be routed as far away as possible from the receiver pins.

## Application Information (continued)

Noise that couples into the receiver through the power supply pins can also degrade performance. It is recommended that the pi filter, shown in Figure 2, be used for both the transmitter and receiver power supplies.

### Data Clock and Signal Detect Outputs

The data clock and signal detect outputs of the 1417 transceiver are driven by open-emitter NPN transistors, which have an output impedance of approximately 7 Ω. Each output can provide approximately 50 mA maximum current to a 50 Ω load terminated to $V_{CC}$ – 2.0 V.

Due to the high switching speeds of ECL outputs, transmission line design must be used to interconnect components. To ensure optimum signal fidelity, both data outputs (RD+/RD–) and clock outputs (CLK+/CLK–) should be terminated identically. The signal lines connecting the data and clock outputs to the next device should be equal in length and have matched impedances. Controlled impedance stripline or microstrip construction must be used to preserve the quality of the signal into the next component and to minimize reflections back into the receiver, which could degrade its performance. Excessive ringing due to reflections caused by improperly terminated signal lines makes it difficult for the component receiving these signals to decipher the proper logic levels and can cause transitions to occur where none were intended. Also, by minimizing high-frequency ringing, possible EMI problems can be avoided.

The signal-detect output is LVTTL logic. A logic low at this output indicates that the optical signal into the receiver has been interrupted or that the light level has fallen below the minimum signal detect threshold. This output should not be used as an error rate indicator, since its switching threshold is determined only by the magnitude of the incoming optical signal.

### Transceiver Processing

When the process plug is placed in the transceiver's optical port, the transceiver and plug can withstand normal wave soldering and aqueous spray cleaning processes. However, the transceiver is not hermetic, and should not be subjected to immersion in cleaning solvents. The transceiver case should not be exposed to temperatures in excess of 125 °C. The transceiver pins can be wave soldered at 250 °C for up to 10 seconds. The process plug should only be used once. After removing the process plug from the transceiver, it must not be used again as a process plug; however, if it has not been contaminated, it can be reused as a dust cover.

## Transceiver Optical and Electrical Characteristics

**Table 2. Transmitter Optical and Electrical Characteristics** ($T_C$ = –40 °C to +85 °C; $V_{CC}$ = 3.135 V to 3.465 V)

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Average Optical Output Power (EOL) | $P_O$ | –15.0 | –8.0 | dBm |
| Optical Wavelength:<br>STM-1 (4 nm spectral width, maximum)<br>STM-4 (2.5 nm spectral width, maximum) | $\lambda_C$ | <br>1261<br>1274 | <br>1360<br>1356 | <br>nm<br>nm |
| Dynamic Extinction Ratio | EXT | 8.2 | — | dB |
| Power Supply Current | $I_{CCT}$ | — | 150 | mA |
| Input Data Voltage:<br>Low<br>High | <br>$V_{IL}$<br>$V_{IH}$ | <br>$V_{CC}$ – 1.81<br>$V_{CC}$ – 1.025 | <br>$V_{CC}$ – 1.62<br>$V_{CC}$ – 0.88 | <br>V<br>V |
| Transmit Disable Voltage | $V_D$ | $V_{CC}$ – 1.3 | $V_{CC}$ | V |
| Transmit Enable Voltage | $V_{EN}$ | $V_{EE}$ | $V_{EE}$ + 0.8 | V |
| Laser Bias Voltage | $V_{BIAS}$ | 0 | 0.70 | V |
| Laser Back-facet Monitor Voltage | $V_{BF}$ | 0.01 | 0.20 | V |

## Transceiver Optical and Electrical Characteristics (continued)

**Table 3. Receiver Optical and Electrical Characteristics** ($T_C$ = –40 °C to +85 °C; $V_{CC}$ = 3.135 V to 3.465 V)

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Average Sensitivity (STM-1/STM-4)* | $P_I$ | — | –28 | dBm |
| Maximum Input Power* | $P_{MAX}$ | –8 | — | dBm |
| Link Status Switching Threshold:<br>Decreasing Light (STM-1/STM-4)<br>Increasing Light (STM-1/STM-4) | <br>$LST_D$<br>$LST_I$ | <br>–45<br>–45 | <br>–29.0<br>–28.5 | <br>dBm<br>dBm |
| Link Status Hysteresis | HYS | 0.5 | — | dB |
| Power Supply Current | $I_{CCR}$ | — | 200 | mA |
| Output Data Voltage/Clock Voltage:<br>Low<br>High | <br>$V_{OL}$<br>$V_{OH}$ | <br>$V_{CC}$ – 1.81<br>$V_{CC}$ – 1.025 | <br>$V_{CC}$ – 1.62<br>$V_{CC}$ – 0.88 | <br>V<br>V |
| Output Data/Clock Rise and Fall Times† | $t_R/t_F$ | 300 | 500 | ps |
| Signal Detect Output Voltage:<br>Low<br>High | <br>$V_{OL}$<br>$V_{OH}$ | <br>0.0<br>2.4 | <br>0.8<br>$V_{CC}$ | <br>V<br>V |
| Clock Duty Cycle | DC | 45 | 55 | % |
| Output Clock Random Jitter | $J_C$ | — | 0.01 | UI |
| Output Clock Random Jitter Peaking | $J_P$ | — | 0.1 | dB |
| Clock/Data Alignment: (See Figure 2.)<br>STM-1<br>STM-4 | TCDA<br><br> | <br>–800<br>–200 | <br>800<br>200 | <br>ns<br>ns |
| Jitter Tolerance/Jitter Transfer | *Telcordia Technologies* GR-253-Core and ITU-TG.958 Compliant | | | |

* For 1 x $10^{-10}$ BER with an optical input using $2^{23}$ – 1 PRBS.
† Typical rise and fall time is 360 ps.

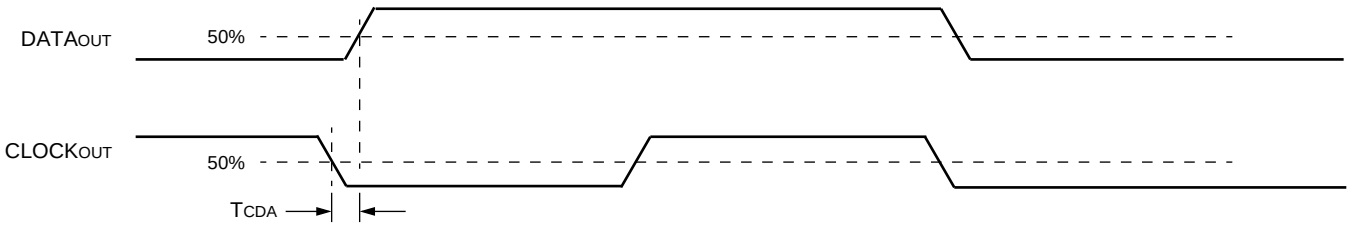



**Figure 2. Clock/Data Alignment**

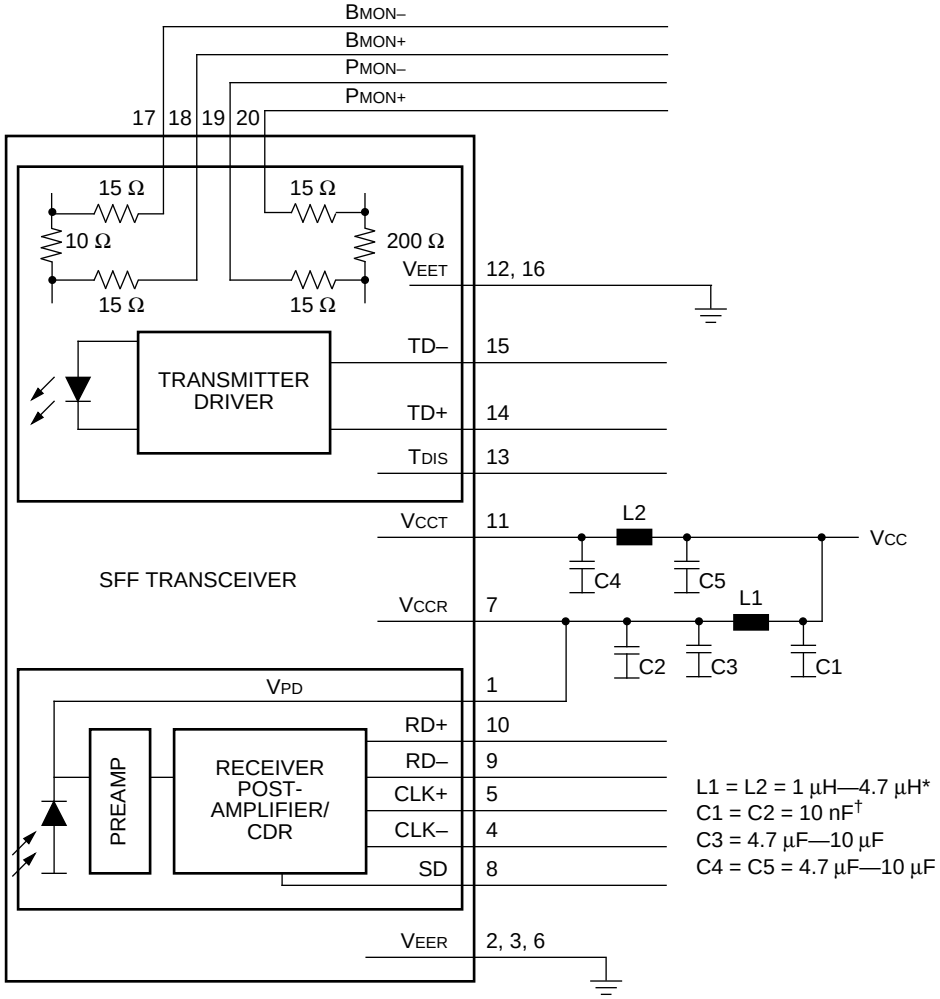
## Qualification and Reliability

To help ensure high product reliability and customer satisfaction, Lucent is committed to an intensive quality program that starts in the design phase and proceeds through the manufacturing process. Optoelectronic modules are qualified to Lucent's internal standards using MIL-STD-883 test methods and procedures and using sampling techniques consistent with *Telcordia Technologies** requirements. The 1417 transceiver is required to pass an extensive and rigorous set of qualification tests.

This qualification program fully meets the intent of Telcordia Technologies reliability practices TR-NWT-000468 and TA-TSY-000983 requirements. In addition, the design, development, and manufacturing facilities of Lucent Technologies Microelectronics Group Optoelectronics unit have been certified to be in full compliance with the latest *ISO*†-9001 quality system standards.

* *Telcordia Technologies* is a trademark of Bell Communications Research, Inc.
† *ISO* is a registered trademark of The International Organization for Standardization.

## Electrical Schematic

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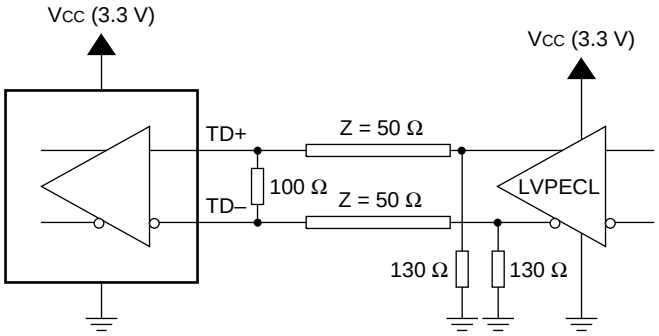
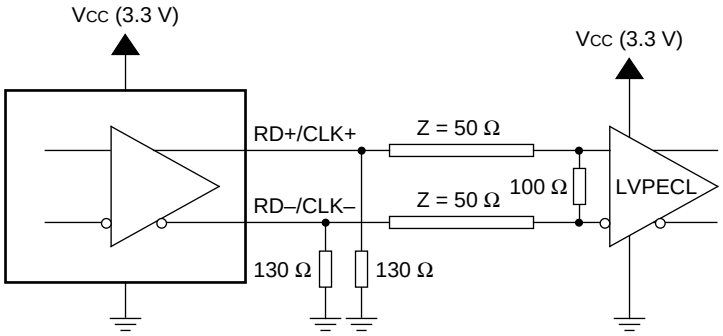
* Ferrite beads can be used as an option.
† For all capacitors, MLC caps are recommended.

**Figure 3. Power Supply Filtering for the Small Form Factor Transceiver**

## Application Schematics




**A. Transmitter Interface (LVPECL to LVPECL)**




**B. Receiver Interface (LVPECL to LVPECL)**

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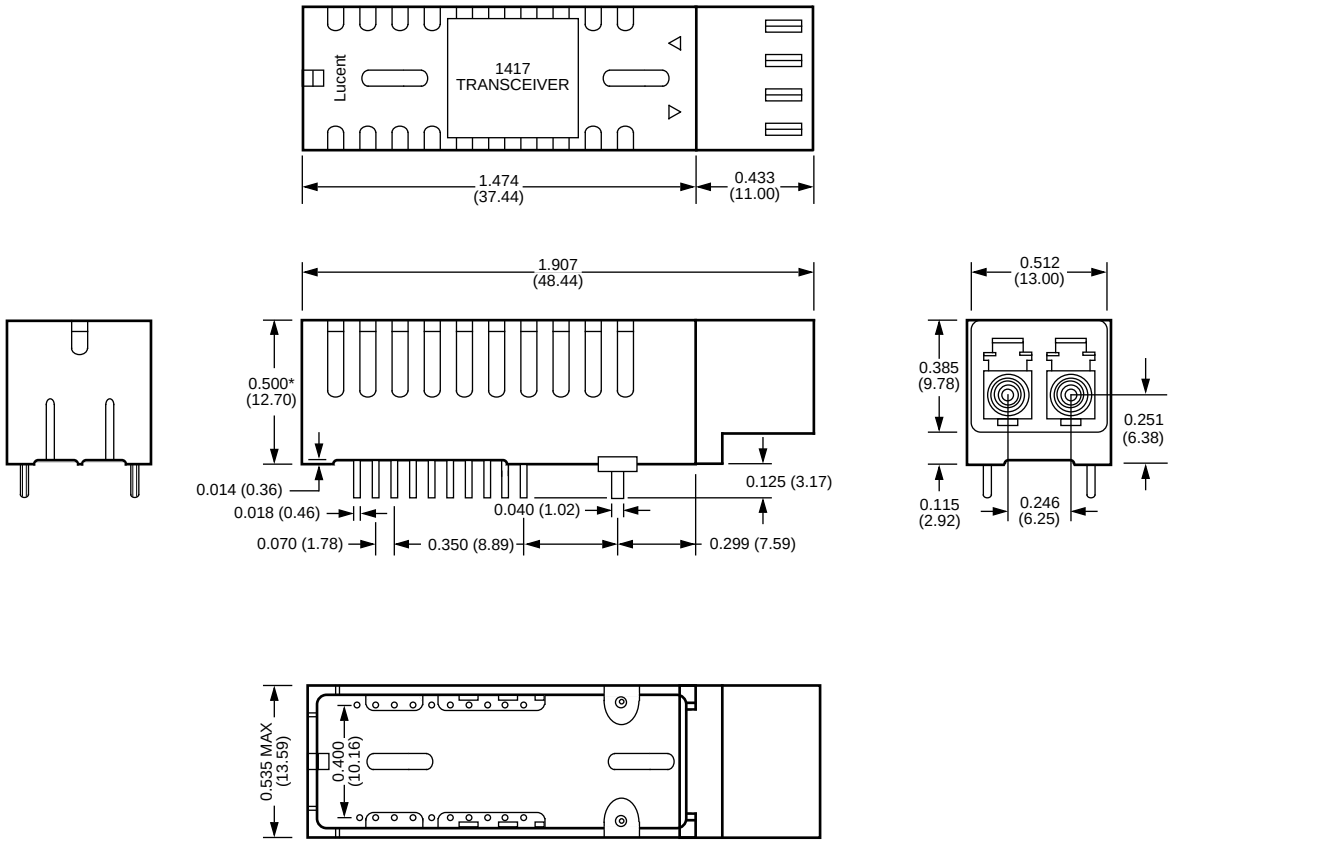
**Figure 4. 3.3 V Transceiver Interface with 3.3 V ICs**

# Outline Diagrams

## Package Outline

Dimensions are in inches and (millimeters).

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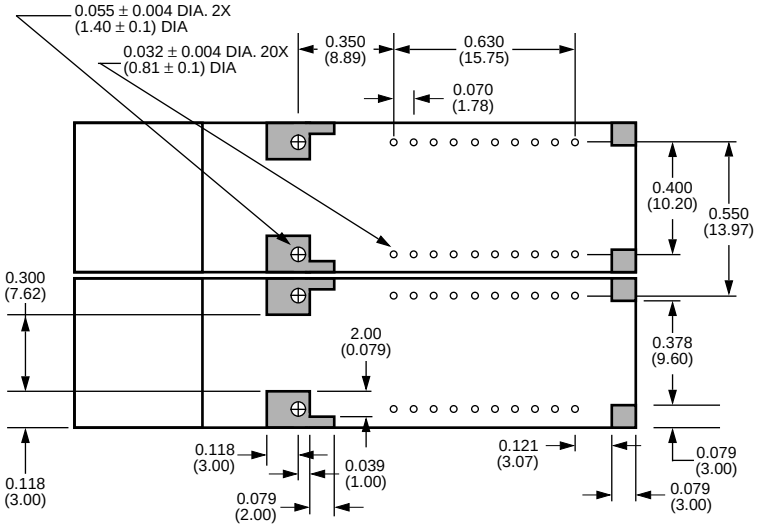
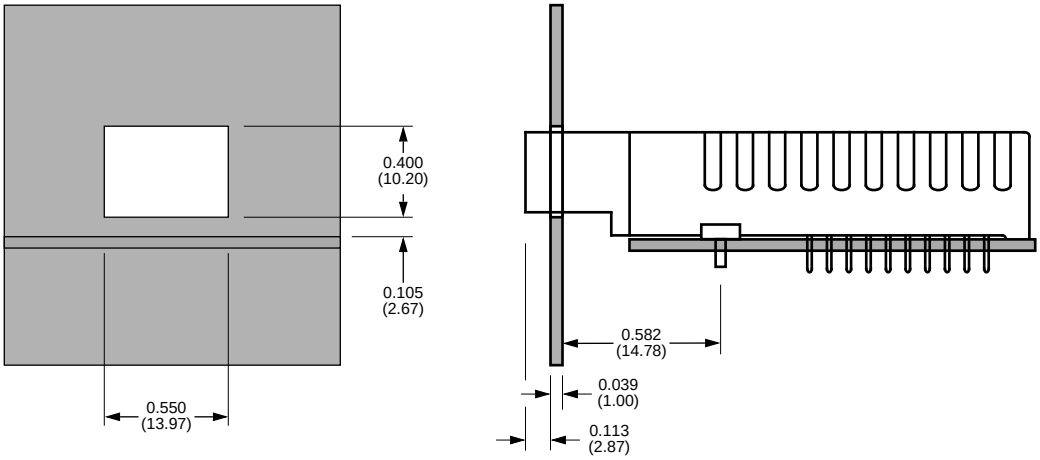
* Dimension does not comply with multisource agreement.

## Outline Diagrams (continued)

### Printed-Wiring Board Layout* and Recommended Panel Opening

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* Per multisource agreement.

# Laser Safety Information

## Class I Laser Product

FDA/CDRH Class I laser product. All versions of the transceiver are Class I laser products per CDRH, 21 CFR 1040 Laser Safety requirements. All versions are Class I laser products per *IEC** 60825-1:1993. The transceiver has been certified with the FDA under accession number 8720009.

**CAUTION: Use of controls, adjustments, and procedures other than those specified herein may result in hazardous laser radiation exposure.**

This product complies with 21 CFR 1040.10 and 1040.11.

Wavelength = 1.3 µm
Maximum power = 0.2 mW

Because of size constraints, laser safety labeling is not affixed to the module but is attached to the outside of the shipping carton.

Product is not shipped with power supply.

* *IEC* is a registered trademark of The International Electrotechnical Commission.

**NOTICE**

**Unterminated optical connectors may emit laser radiation.**

**Do not view with optical instruments.**

# Ordering Information

**Table 4. Ordering Information**

| Description | Device Code | Comcode |
|---|---|---|
| 2 x 10 Single-mode Transceiver for OC-3 /STM-1 (155 Mbits/s) with Clock Recovery | 1417G5A | 108416678 |
| 2 x 10 Single-mode Transceiver for OC-12 /STM-4 (622 Mbits/s) with Clock Recovery | 1417H5A | 108416686 |

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