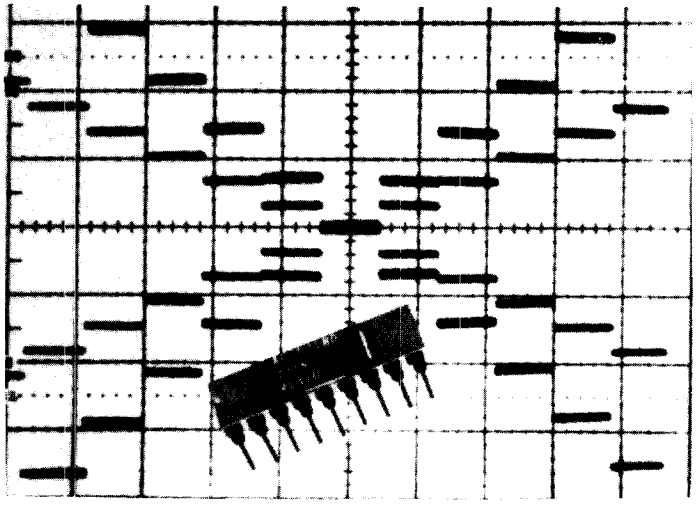
ANALOG DEVICES

CMOS 12-Bit Monolithic Multiplying DAC

AD7541

FEATURES
- Full Four Quadrant Multiplication
- 12-Bit Linearity (0.01%)
- Pretrimmed Gain
- TTL/CMOS Compatible
- Low Power Comsumption
- Low Feedthrough Error
- Low Cost

APPLICATIONS
- Digital/Synchro Conversion
- Programmable Amplifiers
- Ratiometric A/D Conversion
- Function Generation



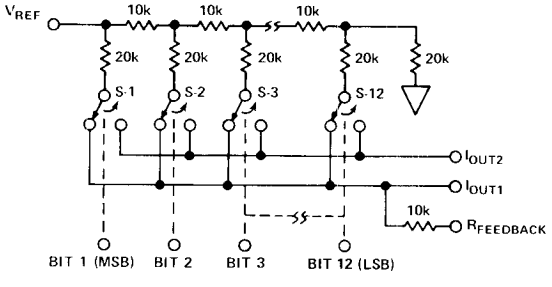
GENERAL DESCRIPTION

The Analog Devices AD7541 is a low cost, high performance 12-bit monolithic multiplying digital-to-analog converter fabricated using advanced double-layer-metal CMOS technology and packaged in a standard 18-pin DIP.

Pin compatible with the AD7521, this new device uses laser wafer trimming to provide full 12-bit linearity and excellent absolute accuracy.

The inherently low power dissipation, coupled with the current switching R-2R ladder, ensures that the performance is maintained over the full temperature range.

FUNCTIONAL DIAGRAM



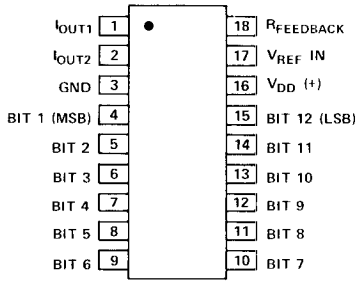
DIGITAL INPUTS (DTL/TTL/CMOS COMPATIBLE)
Logic: A switch is closed to I_{OUT1} for its digital input in a "HIGH" state.

ORDERING INFORMATION

	Temperature Range and Package		
Nonlinearity	Plastic 0 to +70°C	Ceramic -25°C to +85°C	Ceramic -55°C to +125°C
0.02%	AD7541JN	AD7541AD	AD7541SD
0.01%	AD7541KN	AD7541BD	AD7541TD

PIN CONFIGURATION

TOP VIEW



SPECIFICATIONS (V_{DD} = 15V, V_{REF} = +10V unless otherwise noted)

PARAMETER	T_A = +25°C	T_A = min-max	TEST CONDITION
STATIC ACCURACY			
Resolution	12 Bits min	12 Bits min	
Nonlinearity			V_{OUT1} =
AD7541JN, AD7541AD, AD7541SD	±0.02% FSR[1] max	±0.024% FSR max	V_{OUT2} = 0V
AD7541KN, AD7541BD, AD7541TD	±0.01% FSR max	±0.012% FSR max	
Gain Error[1,2]	±0.3% FSR max	±0.4% FSR max	
Power Supply Rejection	±01% per % max	±0.02% per % max	V_{DD} = 14.5V – 15.5V
Output Leakage Current	±50nA max	±200nA max	V_{REF} = ±10V
DYNAMIC PERFORMANCE			
Output Current Settling Time[3]	1µs max	1µs max	To 0.01% of FSR
Feedthrough Error[3]	1mV p-p max	1mV p-p max	V_{REF} = 20V p-p @ 10kHz
REFERENCE INPUT			
Input Resistance	5kΩ min, 20kΩ max	5kΩ min, 20kΩ max	
DIGITAL INPUTS			
V_{INH}	2.4V max	2.4V max	
V_{INL}	0.8V min	0.8V min	
Input Leakage Current	±1µA max	±1µA min	V_{IN} = 0 or 15V
Input Capacitance[3]	8pF max	8pF max	
Input Coding	Binary or Offset Binary		
ANALOG OUTPUTS			
Output Capacitance[3]			
C_{OUT1}	200pF max	200pF max	Digital Inputs
C_{OUT2}	60pF max	60pF max	= V_{INH}
C_{OUT1}	60pF max	60pF max	Digital Inputs
C_{OUT2}	200pF max	200pF max	= V_{INL}
POWER REQUIREMENTS			
V_{DD} Range	+5V min, +16V max	+5V min, +16V max	Accuracy is not guaranteed over this range.
I_{DD}	2mA max	2mA max	Digital Inputs = V_{INH} or V_{INL}

NOTES:
[1] FSR is Full Scale Range.
[2] Using internal feedback resistor.
[3] Guaranteed by design, not subject to test.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} (to GND) . . . . . +17V
V_{REF} (to GND) . . . . . ±25V
Digital Input Voltage Range . . . . . V_{DD} to GND
Output Voltage (Pin 1, Pin 2) . . . . . –100mV to V_{DD}
Power Dissipation (Package)
Up to +75°C 450mW
Derate above +75°C by . . . . . 6mW/°C
Operating Temperature
JN, KN Versions . . . . . 0 to +70°C
AD, BD Versions. . . . . –25°C to +85°C
SD, TD Versions . . . . . –55°C to +125°C
Storage Temperature . . . . . –65°C to +150°C

CAUTION

1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
2. The digital control inputs are zener protected; however permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused inputs in conductive foam at all times.

SPECIFICATION DEFINITIONS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of $(2^{-n})(V_{REF})$. A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the input voltage.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

TYPICAL PERFORMANCE CHARACTERISTICS

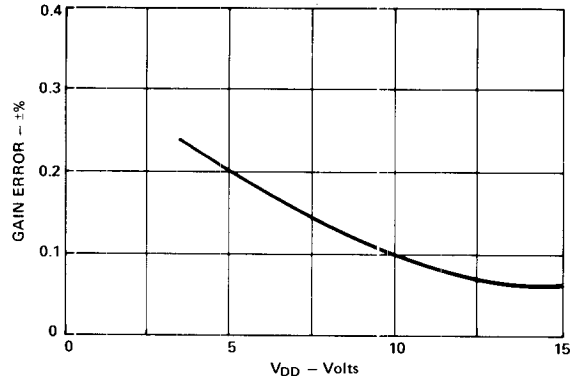


Figure 1. Gain Error vs. Supply Voltage

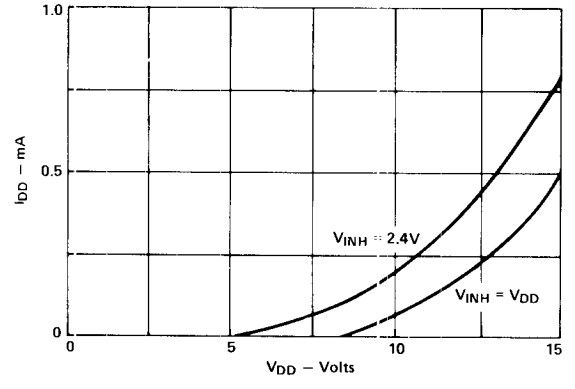


Figure 2. Supply Current vs. Supply Voltage

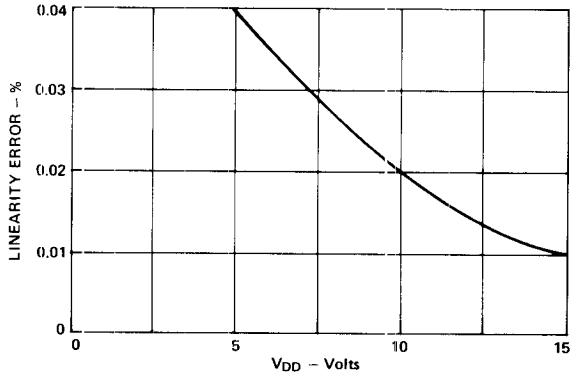


Figure 3. Linearity Error vs. Supply Voltage

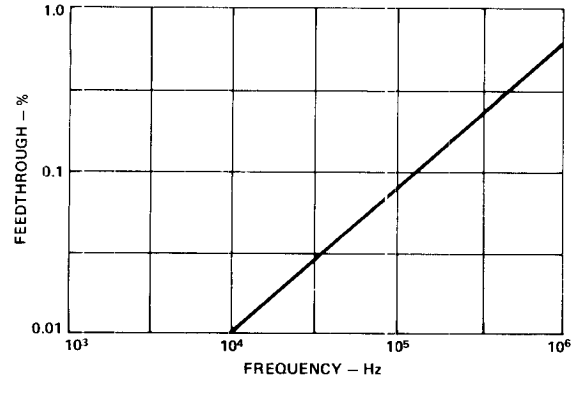


Figure 4. Feedthrough Error vs. Frequency

APPLICATION HINTS

Linearity depends upon the potential of I_{OUT1} and I_{OUT2} (pin 1 and pin 2) being exactly equal to GND (pin 3) and the output amplifiers non-inverting (+) input. Careful PC board layout and adjustment and selection of the amplifiers offset voltage and bias current is necessary.

The input structures of some high speed operational amplifiers can attempt to draw substantial current during switch-on. Schottky diodes should be used in these circumstances to prevent the absolute maximum rating for V_{OUT1} and V_{OUT2} being exceeded.

The power supply should be carefully checked for noise, which would affect performance, and overshoot which could damage the device.

Unused digital inputs must always be grounded or taken to V_{DD} to ensure correct operation. Particular care should be taken when digital inputs are routed to another PC card. It is recommended that inputs open-circuited when PC cards are disconnected be taken to V_{DD} or GND via high value (1MΩ) resistors to prevent the accumulation of static charges.

CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7541, a 12-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and twelve CMOS current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 5. An inverted R-2R ladder structure is used — that is, the binarily weighted currents are switched between the I_{OUT1} and I_{OUT2} bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

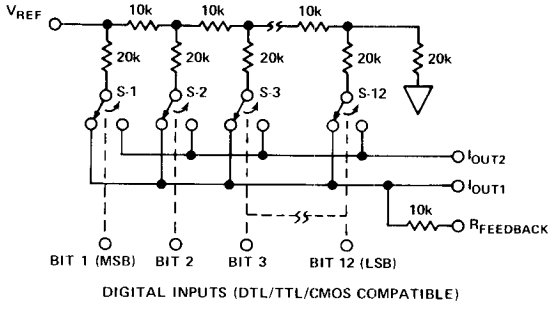


Figure 5. AD7541 Functional Diagram (Inputs "HIGH")

One of the CMOS current switches is shown in Figure 6. The geometries of devices 1, 2 and 3 are optimized to make the digital control inputs DTL/TTL/CMOS compatible over the full military temperature range. The input stage drives two inverters (devices 4, 5, 6 and 7) which in turn drive the two output N-channels. The "ON" resistances of the switches are binarily scaled so the voltage drop across each switch is the same. For example, switch 1 of Figure 6 was designed for an "ON" resistance of 10 ohms, switch 2 of 20 ohms and so on. For a 10V reference input, the current through switch 1 is 0.5mA, the current through switch 2 is 0.25mA, and so on,

thus maintaining a constant 5mV drop across each switch. It is essential that each switch voltage drop be equal if the binarily weighted current division property of the ladder is to be maintained.

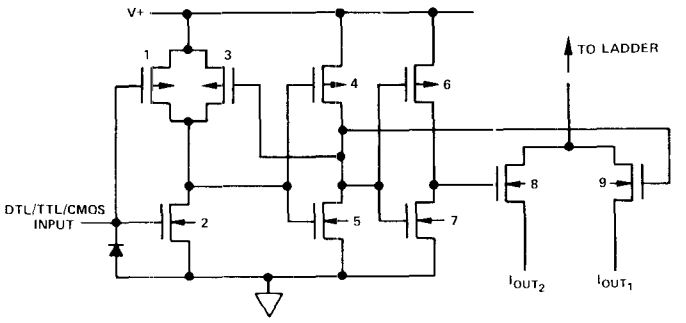


Figure 6. CMOS Switch

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs high and all digital inputs low are shown in Figures 7 and 8. In Figure 7 with all digital inputs low, the reference current is switched to I_{OUT2}. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate while the 1/4096 current source represents a constant 1-bit current drain through the

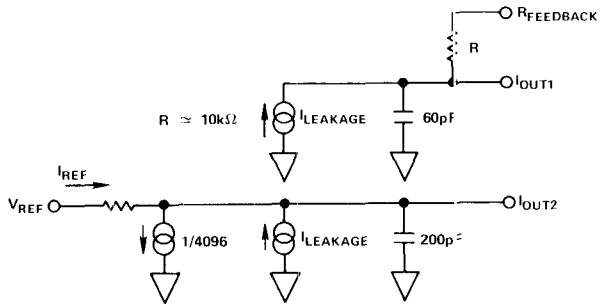


Figure 7. AD7541 Equivalent Circuit – All Digital Inputs Low

termination resistor on the R-2R ladder. The "ON" capacitance of the output N-channel switch is 200pF, as shown on the I_{OUT2} terminal. Analysis of the circuit for all digital inputs high, as shown in Figure 8, is similar to Figure 7; however, the "ON" switches are now on terminal I_{OUT1}, hence the 200pF at that terminal.

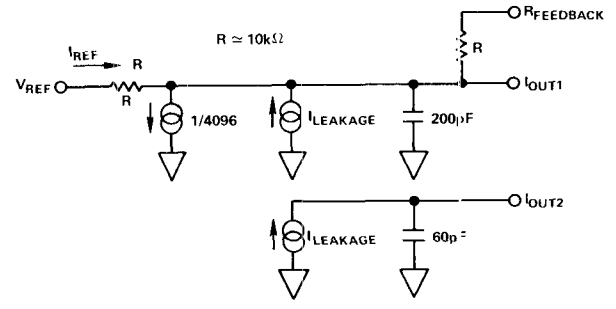


Figure 8. AD7541 Equivalent Circuit – All Digital Inputs High

DYNAMIC PERFORMANCE

OUTPUT IMPEDANCE

The preceding circuit analysis shows that the output capacitance is dependent upon the digital code, as is the output resistance. Looking back into I_{OUT1} the resistance seen is anything between 10kΩ ($R_{FEEDBACK}$ alone) and 5kΩ (R_{FB} in parallel with the 10kΩ network resistance).

This variation affects both static accuracy and dynamic performance. The effect on static accuracy is further considered on the next two pages. The dynamic performance of the AD7541 will depend upon the gain and phase stability of the output amplifier, together with the optimum choice of PC board layout and decoupling components.

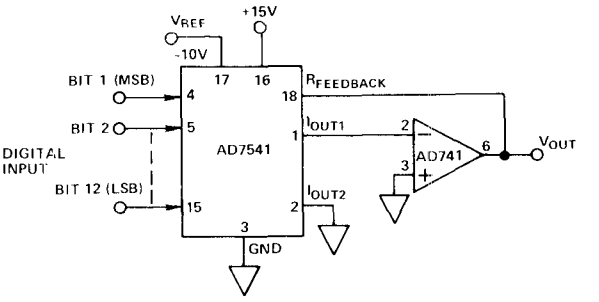


Figure 9. DAC Circuit Using AD741K

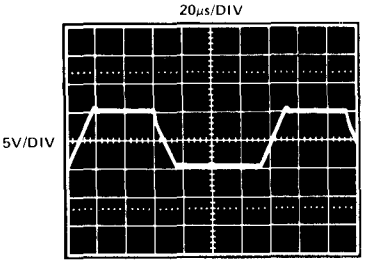


Figure 10. Output Waveform

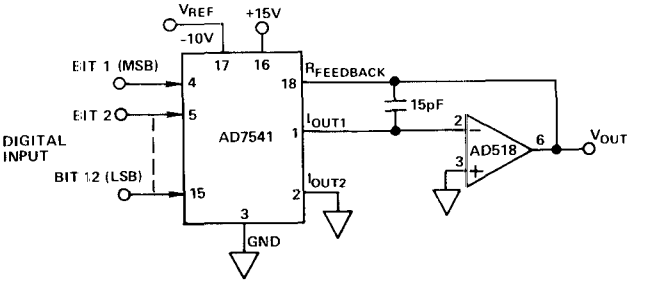


Figure 11. DAC Circuit Using AD518K

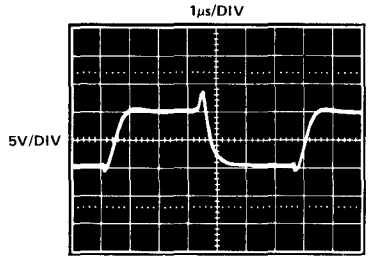


Figure 12. Output Waveform

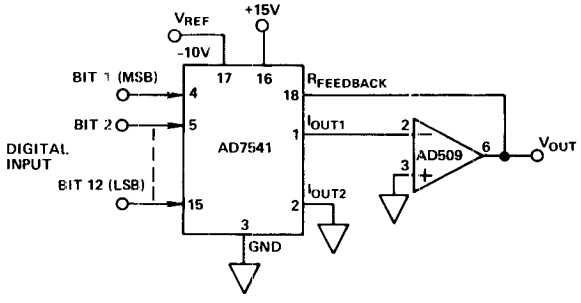


Figure 13. DAC Circuit Using AD509K

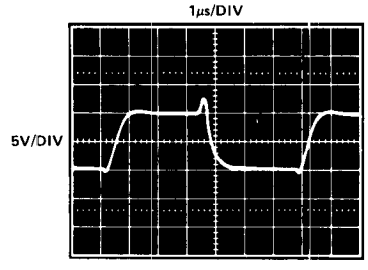


Figure 14. Output Waveform

The circuits and waveforms shown in Figures 9 to 14 are representative of the three principal types of output amplifiers. A general purpose low drift (AD741K), a high speed low cost (AD518), and a fast settling unit (AD509).

Points to remember when applying high speed amplifiers include:

1. Protection diodes as shown in Figures 15 and 16.
2. Phase compensation for the DAC's output capacitance.
3. Power supply decoupling and correct load earthing.

APPLICATIONS

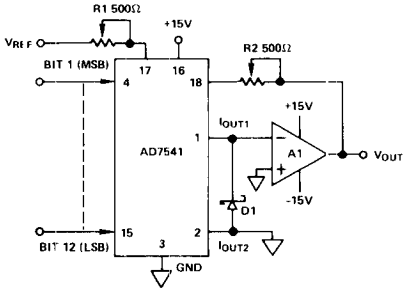


Figure 15. Unipolar Binary Operation

UNIPOLAR BINARY OPERATION

The connections required for unipolar digital binary operation are shown above. V_{REF} may be positive or negative so 2-quadrant multiplication may be performed. Schottky diode D1 (HP 5082-2811 or equivalent) prevents I_{OUT1} from negative excursions which could damage the device. This precaution is only necessary with certain high speed amplifiers.

BIPOLAR (4-QUADRANT) BINARY OPERATION

The digital input is offset binary coded and multiplies V_{REF} according to Table 2. Resistors R1 and R2 should be equal within 0.1% at all temperatures, but need not track the resistors within the AD7541. D1 and D2 perform the same

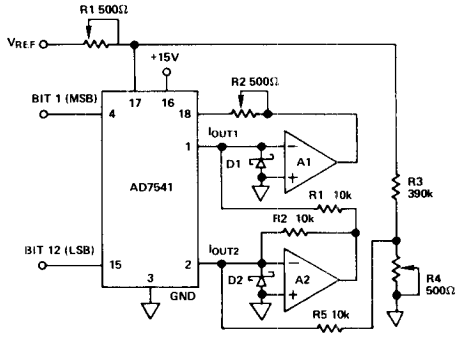


Figure 16. Bipolar (4-Quadrant) Binary Operation

function as in Figure 15. Network R3, R4, R5 sum ½LSB of current into I_{OUT2} to ensure correct coding at zero.

R1 or R2 can be adjusted to produce the outputs shown in Table 1. However, it is recommended that when the application permits it R1 and R2 be omitted. The maximum gain error in this condition is 0.3% of full scale. The offset voltage of amplifier A1 should be adjusted to less than 0.5mV over the temperature range.

DIGITAL INPUT	NOMINAL ANALOG OUTPUT
111111111111	-0.99975 V_{REF}
100000000000	-0.50000 V_{REF}
010000000000	-0.49975 V_{REF}
000000000000	0

Table 1. Code Table for Circuit of Figure 15.

DIGITAL INPUT	NOMINAL ANALOG OUTPUT
111111111111	-0.99951 V_{REF}
100000000001	-0.00049 V_{REF}
100000000000	0
010000000000	+0.50000 V_{REF}
000000000000	+1.00000 V_{REF}

Table 2. Code Table for Circuit of Figure 16.

Amplifiers A1 and A2 should be adjusted to an input offset of less than 0.1mV and should be better than 0.5mV over the temperature range. With V_{REF} set to approximately 10V, R4 should be adjusted so that with code 100000000000 V_{OUT} = 0V ±0.2mV. R1 or R2 should be adjusted so that with code 000000000000 $V_{OUT} = V_{REF}$.

As with the unipolar circuit R1 and R2 can be omitted, with a resulting maximum gain error of 0.3% of full scale. R4 may be replaced by a 100Ω fixed resistor. The maximum zero error if this is done is 0.015% of F.S.R.

OUTPUT AMPLIFIER CONSIDERATIONS

It has already been pointed out that the DAC output resistance varies with the digital code. The effect this has on static accuracy will now be considered.

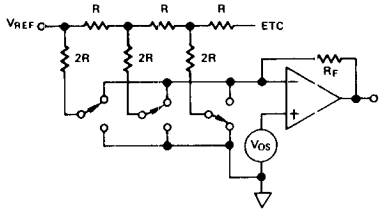


Figure 17.

$$\text{The error voltage} = V_{OS}\left(1 + \frac{R_F}{R_O}\right)$$

R_O is a function of the digital code.
$R_O \cong 10k\Omega$ for any more than 4-bits Logic 1.
$R_O \cong 30k\Omega$ for any single bit Logic 1.

The gain for offset, therefore, changes as follows:

$$\text{At code 001111111111 } V_{ERROR1} = V_{OS}\left(1 + \frac{10k}{10k}\right) = 2\ V_{OS}$$

$$\text{At code 010000000000 } V_{ERROR2} = V_{OS}\left(1 + \frac{10k}{30k}\right) = \frac{4}{3}\ V_{OS}$$

The error difference is therefore $\frac{2}{3}\ V_{OS}$

Since, for a 12-bit resolution DAC, one LSB has a weight (for V_{REF} = +10V) of 2.5mV, it is clearly important that V_{OS} be nulled, either using the amplifiers nulling facility or an external network.

It is important to realize that an offset can be caused by including the usual bias current compensation resistor in the amplifiers non-inverting input terminal. This should not be included. Instead the amplifier should have a bias current which is low over the temperature range of interest, and should certainly not exceed 75nA.

ANALOG/DIGITAL DIVISION

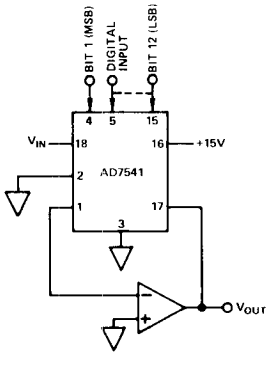


Figure 18. Analog/Digital Divider

With the AD7541 connected in its normal multiplying configuration as shown in Figure 15, the transfer function is

$$V_O = -V_{IN}\left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \ldots\ldots \frac{A_{12}}{A^{12}}\right)$$

where the coefficients A_X assume a value of 1 for an ON bit and 0 for an OFF bit.

By connecting the DAC in the feedback of an operational amplifier, as shown in Figure 18, the transfer function becomes

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \ldots\ldots \frac{A_{12}}{A^{12}}}\right)$$

This is division of an analog variable (V_{IN}) by a digital word. With all bits off, the amplifier saturates to its bound, since division by zero is not defined. With the LSB (Bit 12) ON, the gain is 4096. With all bits ON, the gain is 1 (±1 LSB).

DIGITAL/SYNCHRO CONVERTER

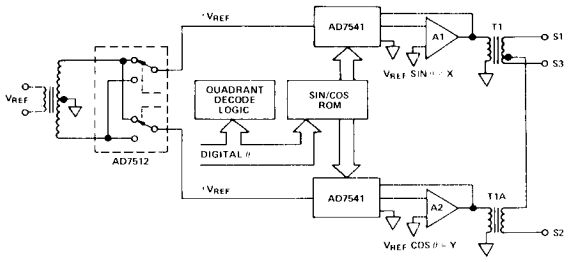


Figure 19. 14-Bit Digital to Synchro Converter

The low cost and high accuracy available from the AD7541, together with its bipolar multiplying capability is exploited fully in the circuit of Figure 19. V_{REF} is commonly 400Hz but by replacing the transformers with dc coupled circuits coordinate transformation may be performed.

The SIN/COS ROM is readily available at low cost and the AD7512 switch enables greater resolution to be obtained.

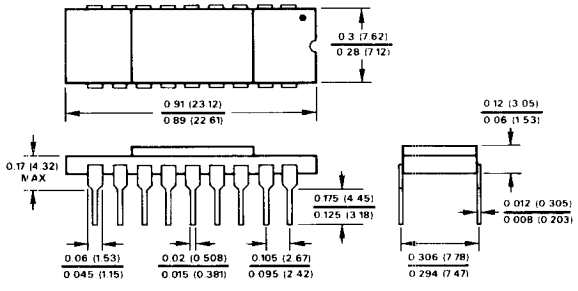
Resolver-to-synchro transformation is performed by the Scott connected pair T1 and T1A. The power available to the load connected to S1, S2 and S3 is determined by the amplifiers A1 and A2. A particular advantage of the circuit shown in Figure 19 is that it is invariant with respect to θ, and may be used to directly drive equipment such as CRT displays.

MECHANICAL INFORMATION

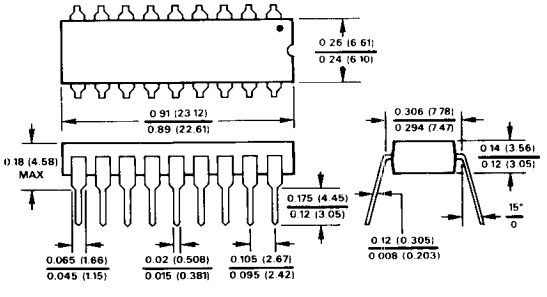
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

18 PIN CERAMIC DIP



18 PIN PLASTIC DIP



BONDING DIAGRAM