8K-bit TTL bipolar PROM (1024x8) 82S181A

FEATURES

- Address access time: 55ns max
- Input loading: -150µA max
- On-chip address decoding
- Four chip enable inputs
- Outputs: 3-State
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible

APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

DESCRIPTION

The 82S181A is field-programmable, which means that custom patterns are immediately available by following the Philips Generic I fusing procedure. The 82S181A is supplied with all outputs at a logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 4 chip enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

ORDERING INFORMATION

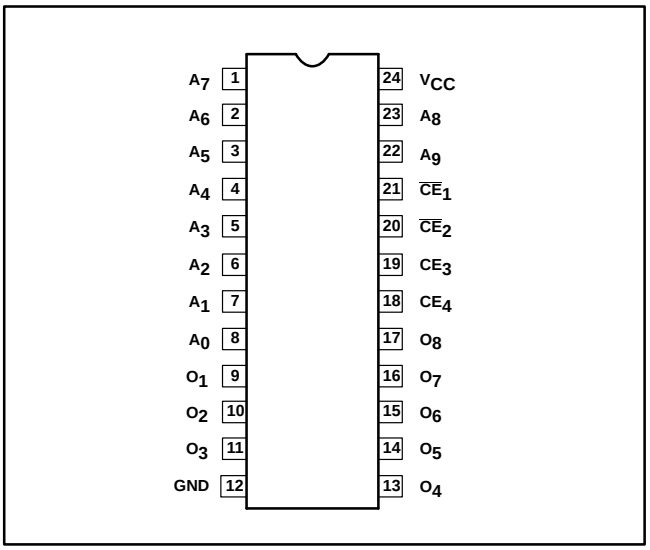
DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
24-pin Ceramic DIP (600mil-wide)	82S181A/BJA	GDIP1-T24
24-pin Ceramic Flat Pack	82S181A/BKA	GDFP2-F24
28-Pin Ceramic LLCC	82S181A/B3A	CQCC2-N28

* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

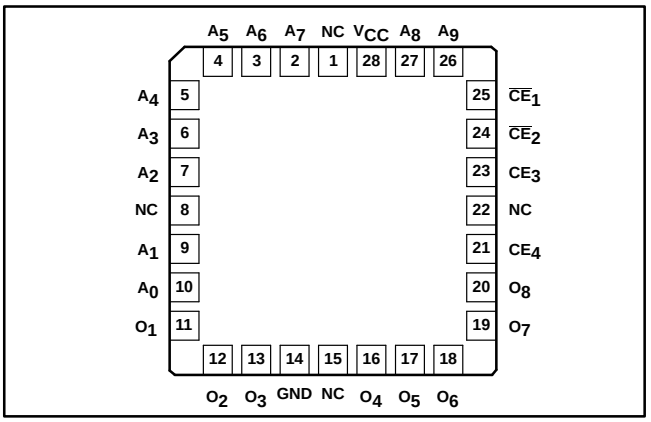
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_I	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_A	Operating temperature range	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



LLCC LEAD CONFIGURATION



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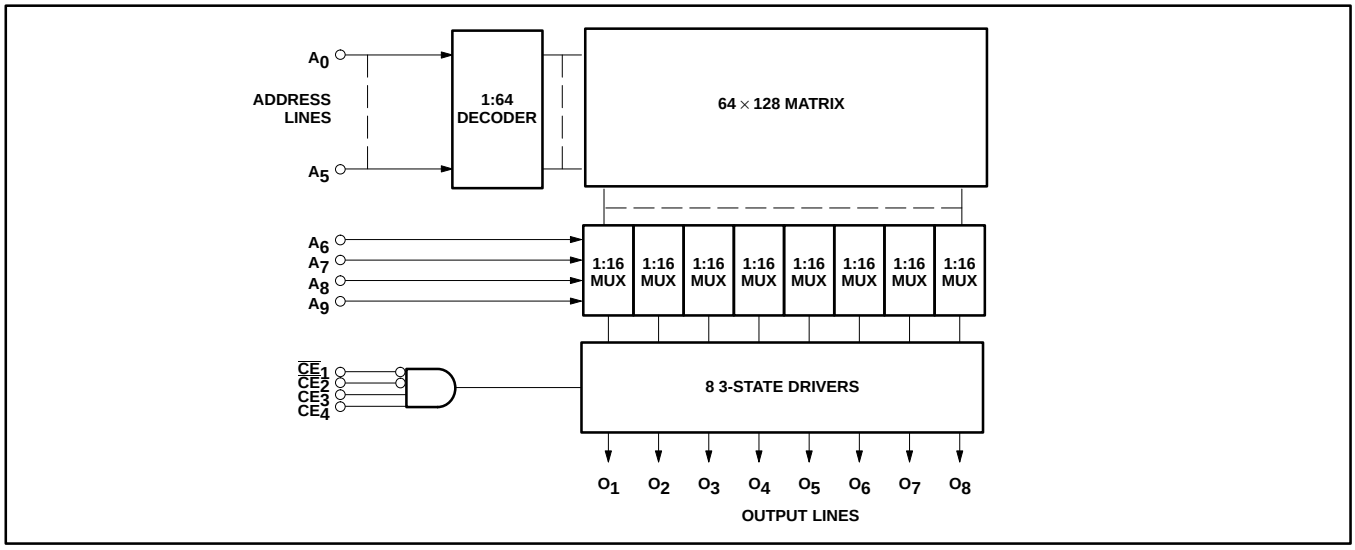
BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS $-55^{\circ}C \leq T_A \leq +125^{\circ}C$, $4.5V \leq V_{CC} \leq 5.5V$

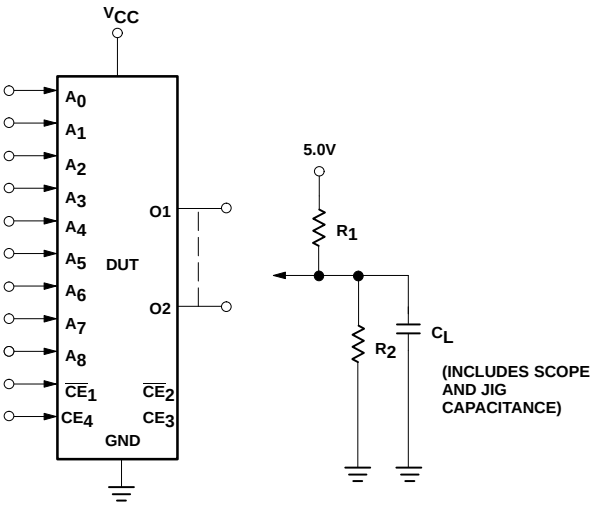
SYMBOL	PARAMETER	TEST CONDITIONS[1, 2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage[2]						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IK}	Clamp	V_{CC} = 4.5V, I_I = -18mA		-0.8	-1.2	V
Output voltage[2]						
		V_{CC} = 4.5V, $\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High				
V_{OL}	Low	I_O = 9.6mA			0.5	V
V_{OH}	High	I_O = -2mA	2.4			V
Input current[1]						
		V_{CC} = 5.5V				
I_{IL}	Low	V_I = 0.45V			-150	µA
I_{IH}	High	V_I = 5.5V			40	µA
Output current[1]						
		V_{CC} = 5.5V				
I_{OZ}	Hi-Z state	$\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low, V_O = 5.5V			40	µA
		$\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low, V_O = 0.4V			-40	µA
I_{OS}	Short circuit[3]	$\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High, V_O = 0V	-15		-85	mA
		V_{CC} = 5.5V, High stored				
Supply current						
I_{CC}		$\overline{CE}_{1,2}$ = High, $\overline{CE}_{3,4}$ = Low, V_{CC} = 5.5V		125	185	mA
Capacitance[6]						
		$\overline{CE}_{1,2}$ = High, V_{CC} = 5.0V				
C_{IN}	Input	V_I = 2.0V		5	10	pF
C_{OUT}	Output	V_O = 2.0V		8	13	pF

AC ELECTRICAL CHARACTERISTICS $-55^{\circ}C \leq T_A \leq +125^{\circ}C$, $4.5V \leq V_{CC} \leq 5.5V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
t_{AA}	Access time[4]	Output	Address		45	55	ns
t_{CE}	Access time[4]	Output	Chip Enable		25	40	ns
t_{CD}	Disable time	Output	Chip Disable		25	40	ns

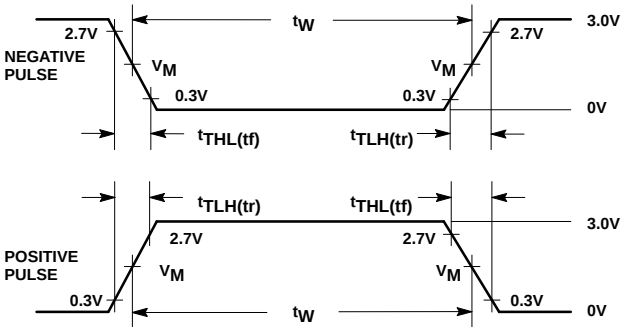
NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1µs.
5. Typical values are at V_{CC} = 5V, T_A = +25°C.
6. Guaranteed, but not tested.

TEST LOAD CIRCUITS



NOTE: R_1 = 470Ω, R_2 = 1KΩ, C_L = 50pF.

VOLTAGE WAVEFORMS



Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

TIMING DIAGRAMS