HARRIS SEMICONDUCTOR

RFP42N03L, RF1S42N03L, RF1S42N03LSM

42A, 30V, 0.025Ω, N-Channel Logic Level Power MOSFETs

March 1997

Features

- **42A, 30V**
- **$r_{DS(ON)}$ 0.025Ω**
- ***Temperature Compensating* PSPICE Model**
- **Can be Driven Directly from CMOS, NMOS, and TTL Circuits**
- **Peak Current vs Pulse Width Curve**
- **UIS Rating Curve**
- **175°C Operating Temperature**

Ordering Information

PART NUMBER	PACKAGE	BRAND
RFP42N03L	TO-220AB	FP42N03L
RF1S42N03L	TO-262AA	F42N03L
RF1S42N03LSM	TO-263AB	F42N03L

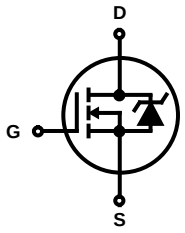
NOTE: When ordering, use the entire part number. Add the suffix, 9A, to obtain the TO-263AB variant in tape and reel, e.g. RF1S42N03LSM9A.

Description

The RFP42N03L, RF1S42N03L, and RF1S42N03LSM are N-Channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers and relay drivers. These transistors can be operated directly from integrated circuits.

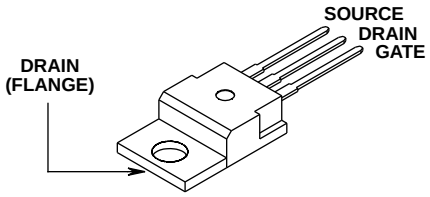
Formerly developmental type TA49030.

Symbol

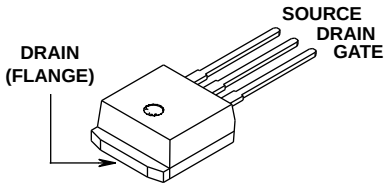


Packaging

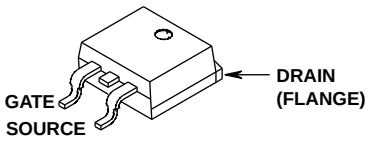
JEDEC TO-220AB



JEDEC TO-262AA



JEDEC TO-263AB



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **4302**

Absolute Maximum Ratings $T_C = 25^oC$

		RFP42N03L, RF1S42N03L, RF1S42N03LSM	UNITS
Drain to Source Voltage	V_{DSS}	30	V
Drain to Gate Voltage (R_{GS} = 20KΩ)	V_{DGR}	30	V
Gate to Source Voltage	V_{GS}	±10	V
Drain Current			
Continuous	I_D	42	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation	P_D	90	W
Derate Above 25^oC		0.606	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^oC
Soldering Temperature of Leads for 10s	T_L	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V		30	-	-	V
Gate to Source Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA		1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30V, V_{GS} = 0V	$T_C = 25^oC$	-	-	1	μA
			$T_C = 150^oC$	-	-	50	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±10V		-	-	100	nA
Drain to Source On Resistance	$r_{DS(ON)}$	I_D = 42A, V_{GS} = 5V		-	-	0.025	Ω
Turn-On Time	t_{ON}	V_{DD} = 15V, $I_D \cong$ 42A, R_L = 0.357Ω, V_{GS} = 5V, R_{GS} = 5Ω		-	-	260	ns
Turn-On Delay Time	$t_{d(ON)}$			-	15	-	ns
Rise Time	t_r			-	160	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	20	-	ns
Fall Time	t_f			-	20	-	ns
Turn-Off Time	t_{OFF}			-	-	60	ns
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0V to 10V	V_{DD} = 24V, $I_D \cong$ 42A, R_L = 0.571Ω	-	50	60	nC
Gate Charge at 5V	$Q_{g(5)}$	V_{GS} = 0V to 5V		-	30	36	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0V to 1V		-	1.5	1.8	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	1650	-	pF
Output Capacitance	C_{OSS}			-	575	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	200	-	pF
Thermal Resistance Junction-to-Case	$R_{\theta JC}$			-	-	1.65	$^oC/W$
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$			-	-	80	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Forward Voltage	V_{SD}	I_{SD} = 42A	-	-	1.5	V
Reverse Recovery Time	t_{rr}	I_{SD} = 42A, dI_{SD}/dt = 100A/μs	-	-	125	ns

Typical Performance Curves Unless Otherwise Specified

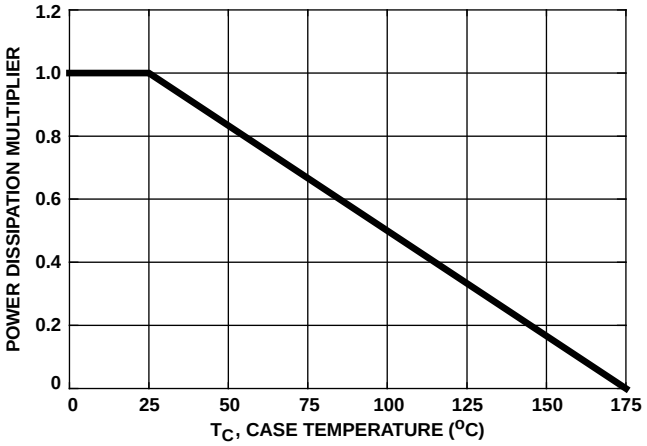


FIGURE 1. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

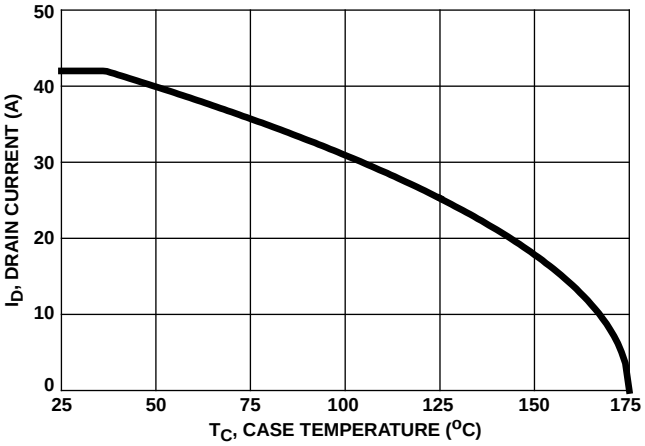


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

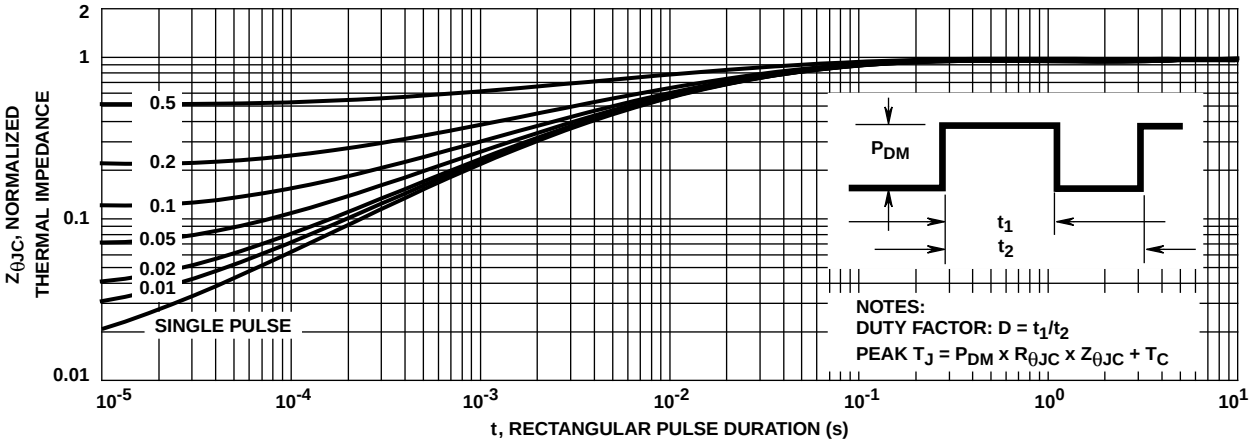


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

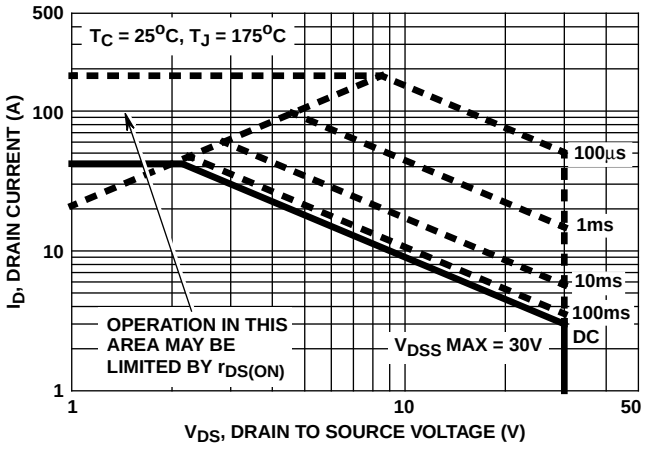


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

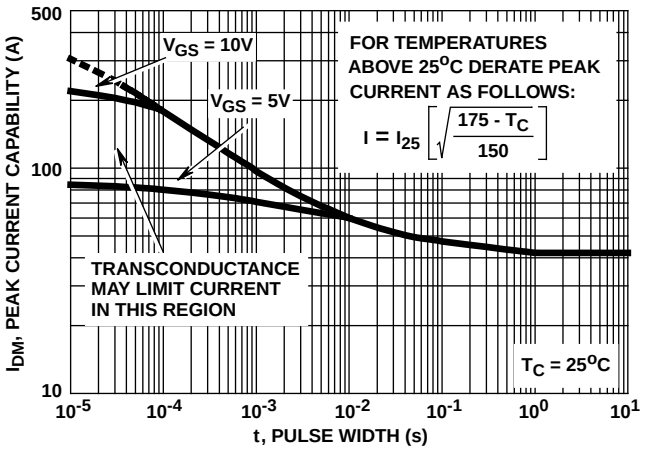
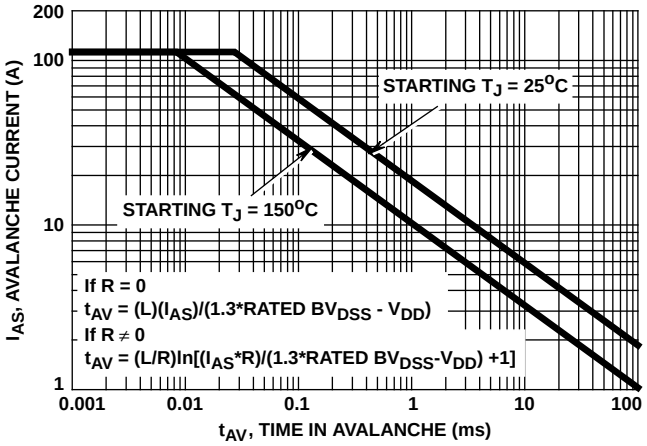


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves Unless Otherwise Specified (Continued)



NOTE: Refer to Harris Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING

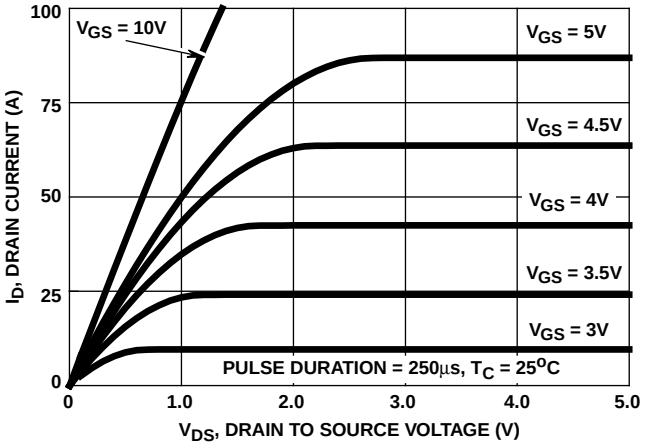


FIGURE 7. SATURATION CHARACTERISTICS

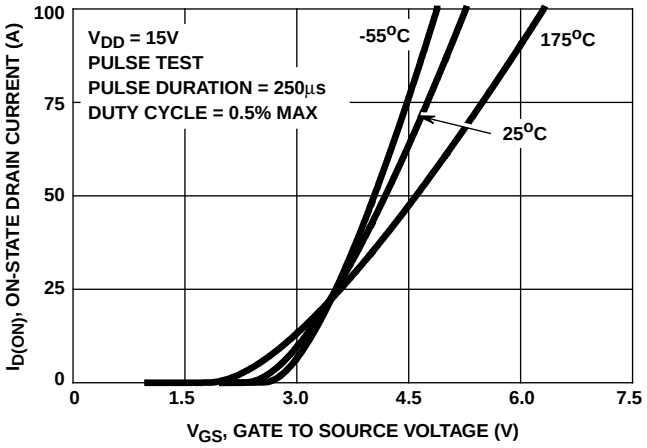


FIGURE 8. TRANSFER CHARACTERISTICS

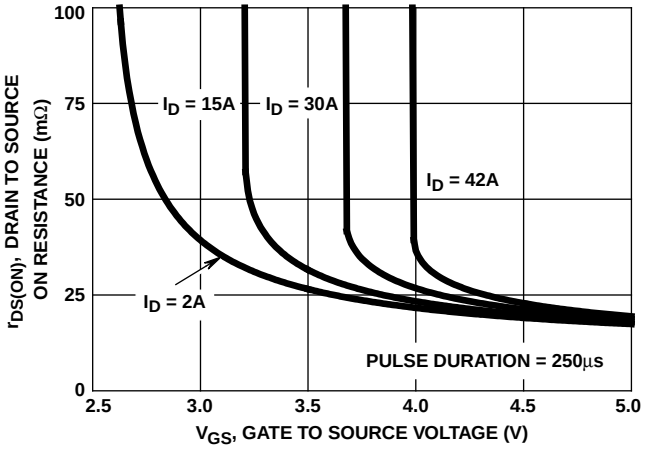


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE FOR VARYING CONDITIONS OF GATE VOLTAGE AND DRAIN CURRENT

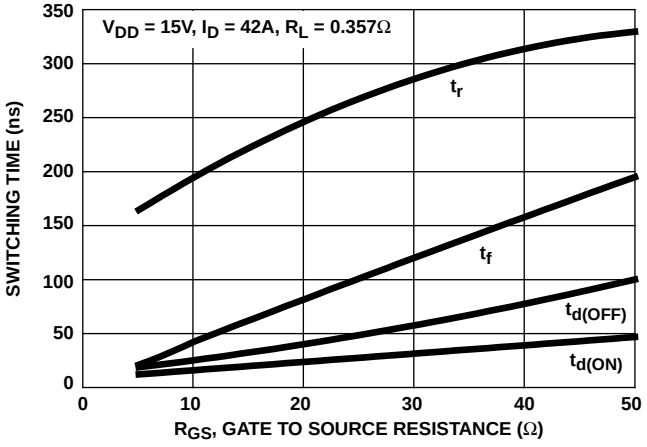


FIGURE 10. SWITCHING TIME AS A FUNCTION OF GATE RESISTANCE

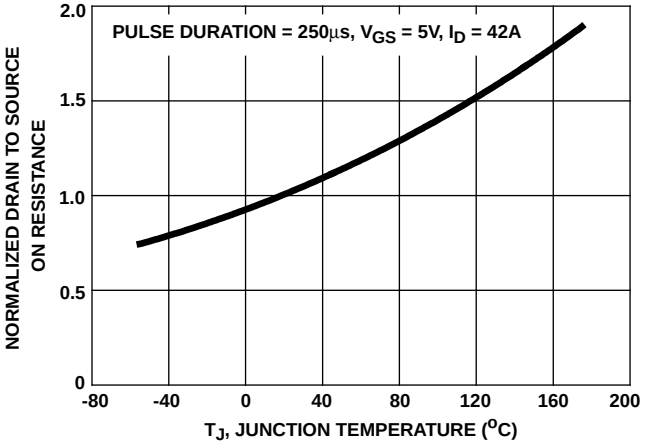


FIGURE 11. DRAIN TO SOURCE NORMALIZED ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

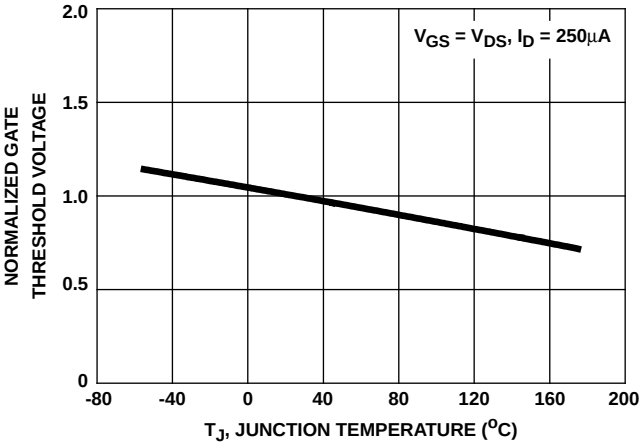


FIGURE 12. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

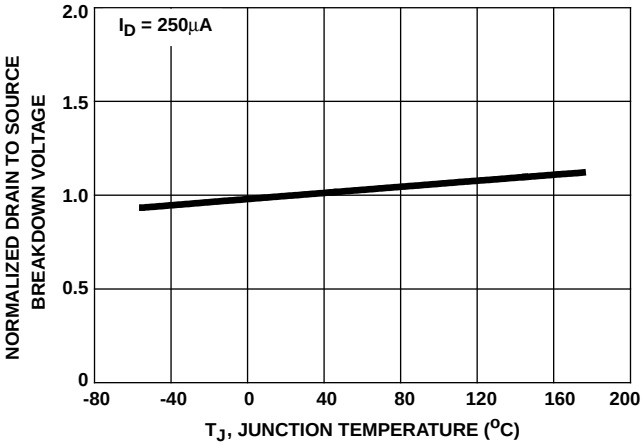


FIGURE 13. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

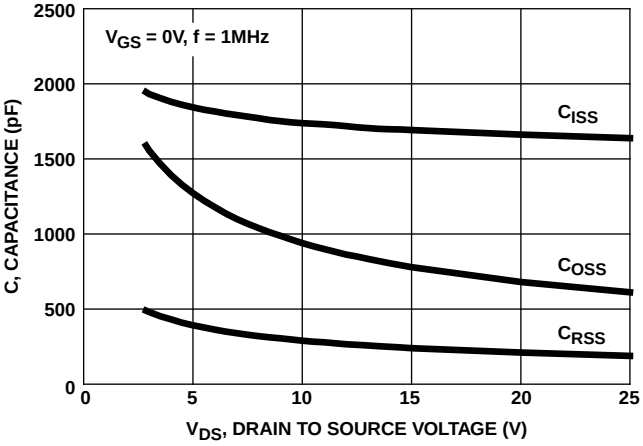
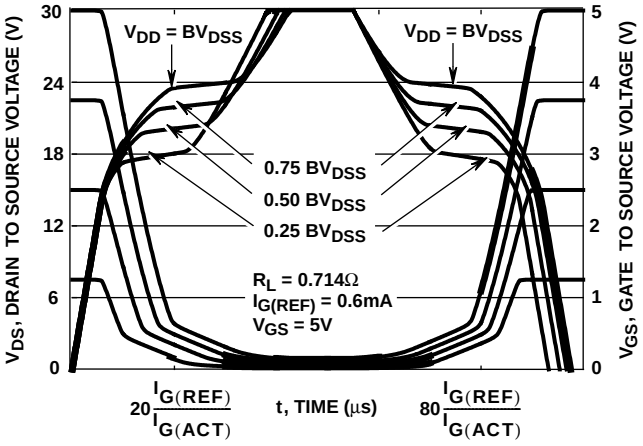


FIGURE 14. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Application Notes AN7254 and AN7260.

FIGURE 15. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

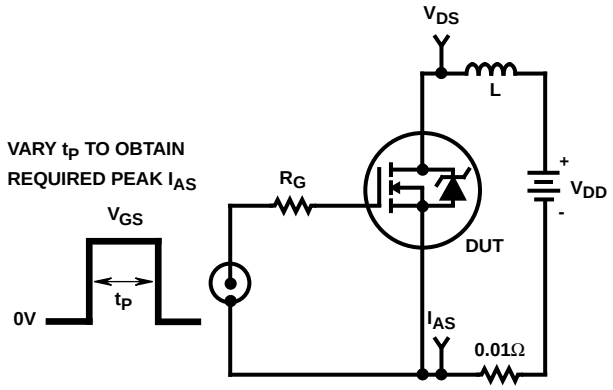


FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

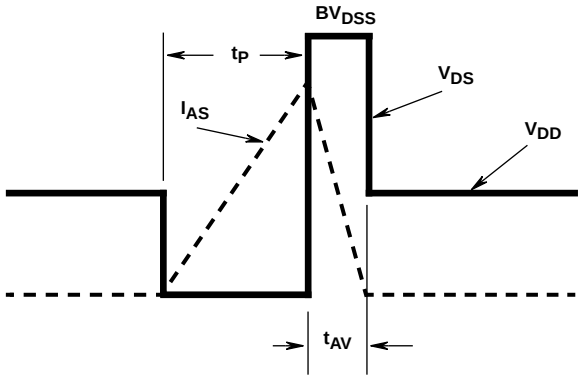


FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

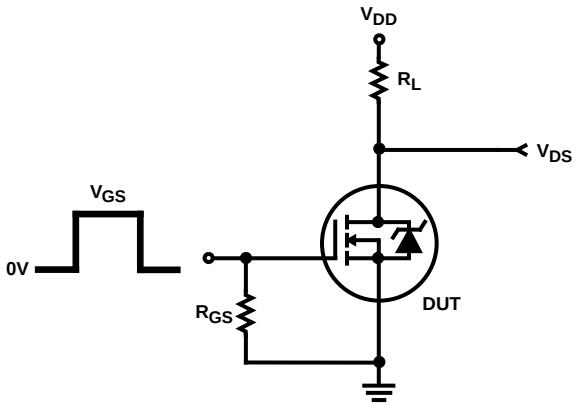


FIGURE 18. RESISTIVE SWITCHING TEST CIRCUIT

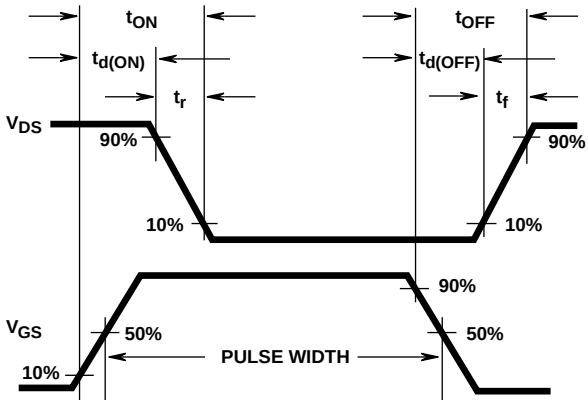


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

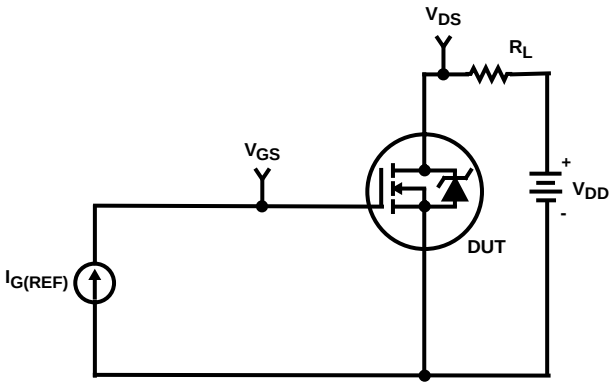


FIGURE 20. GATE CHARGE TEST CIRCUIT

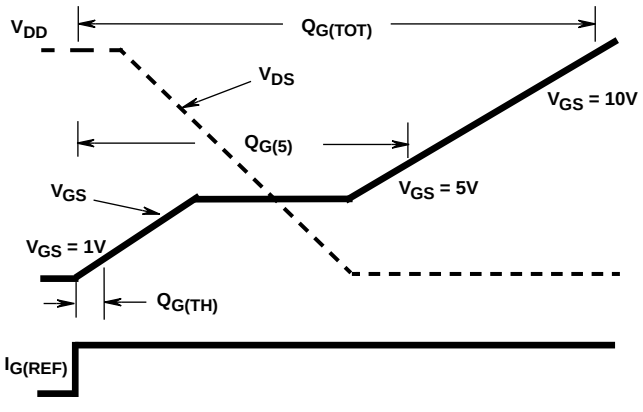


FIGURE 21. GATE CHARGE WAVEFORMS

Temperature Compensated PSPICE Model for the RFP42N03L, RF1S42N03L, RF1S42N03LSM

.SUBCKT RFP42N03L 2 1 3 ; rev 12/24/96

CA 12 8 2.55e-9
CB 15 14 2.64e-9
CIN 6 8 1.45e-9

DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD

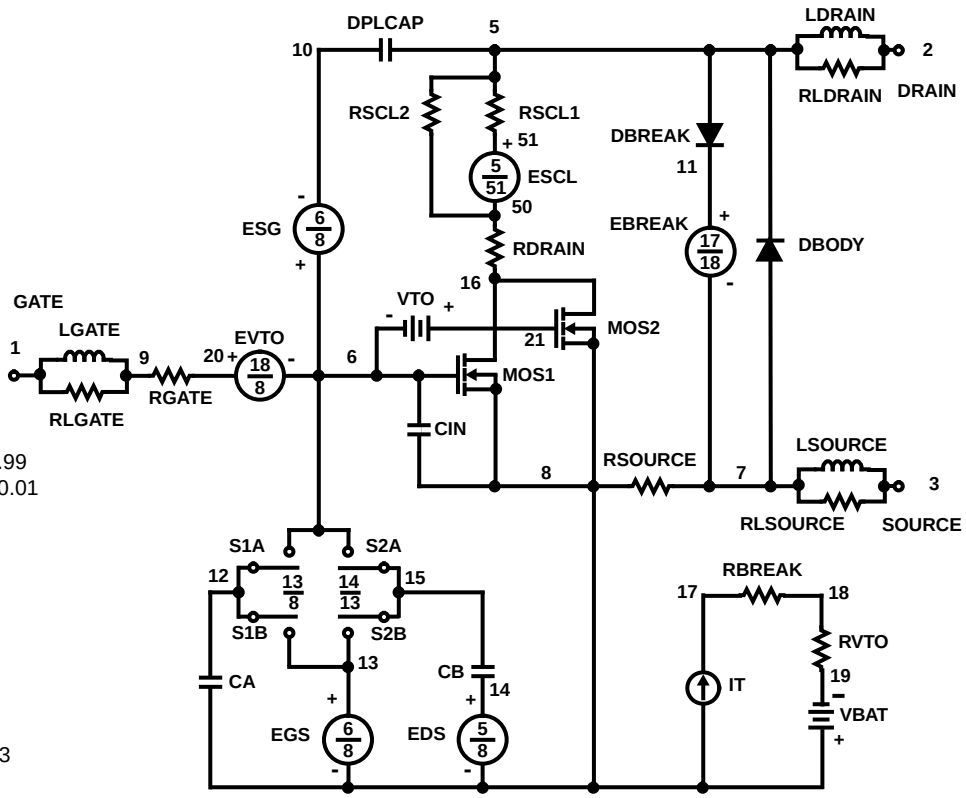
EBREAK 11 7 17 18 33.3
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 4.9e-9
LSOURCE 3 7 4.9e-9

MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 0.14e-3
RGATE 9 20 0.89
RLDRAIN 2 5 10
RLGATE 1 9 49
RLSOURCE 3 7 49
RSCL1 5 51 RSCLMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RDSMOD 10.31e-3
RVTO 18 19 RVTOMOD 1



S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.583

ESCL 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/176,6))}

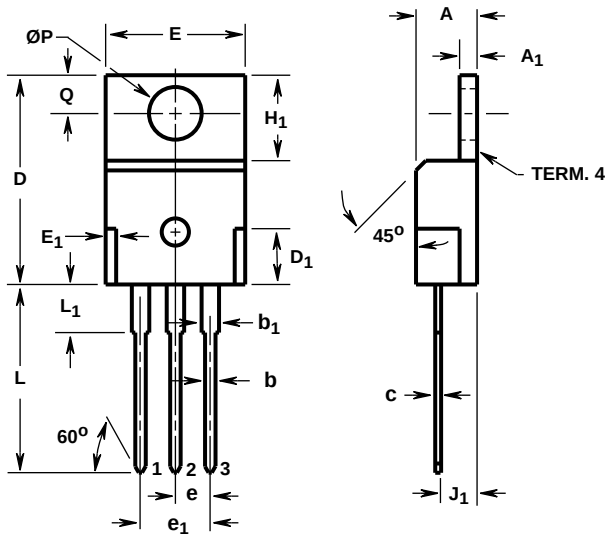
.MODEL DBDMOD D (IS = 3.61e-13 RS = 5.06e-3 TRS1 = 3.05e-3 TRS2 = 7.57e-6 CJO = 2.16e-9 TT = 2.18e-8)
.MODEL DBKMOD D (RS = 1.66e-1 TRS1 = -2.97e-3 TRS2 = 7.57e-6)
.MODEL DPLCAPMOD D (CJO = 0.96e-9 IS = 1e-30 N = 10)
.MODEL MOSMOD NMOS (VTO = 2.313 KP = 53.82 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBKMOD RES (TC1 = 8.95e-4 TC2 = -1e-7)
.MODEL RDSMOD RES (TC1 = 3.82e-3 TC2 = 1.17e-5)
.MODEL RSCLMOD RES (TC1 = 2.03e-3 TC2 = 0.45e-5)
.MODEL RVTOMOD RES (TC1 = -2.27e-3 TC2 = -5.75e-7)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.82 VOFF= -2.82)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.82 VOFF= -4.82)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.67 VOFF= 2.33)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 2.33 VOFF= -2.67)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.

TO-220AB

3 LEAD JEDEC TO-220AB PLASTIC PACKAGE



Lead No. 1	-	Gate
Lead No. 2	-	Drain
Lead No. 3	-	Source
Term. 4 Mounting Flange	-	Drain

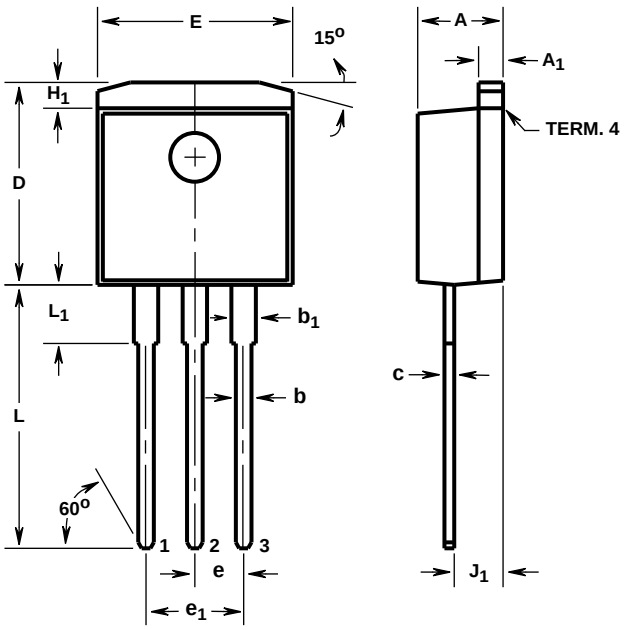
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	-
b	0.030	0.034	0.77	0.86	3, 4
b_1	0.045	0.055	1.15	1.39	2, 3
c	0.014	0.019	0.36	0.48	2, 3, 4
D	0.590	0.610	14.99	15.49	-
D_1	-	0.160	-	4.06	-
E	0.395	0.410	10.04	10.41	-
E_1	-	0.030	-	0.76	-
e	0.100 TYP		2.54 TYP		5
e_1	0.200 BSC		5.08 BSC		5
H_1	0.235	0.255	5.97	6.47	-
J_1	0.100	0.110	2.54	2.79	6
L	0.530	0.550	13.47	13.97	-
L_1	0.130	0.150	3.31	3.81	2
ØP	0.149	0.153	3.79	3.88	-
Q	0.102	0.112	2.60	2.84	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Lead dimension and finish uncontrolled in L_1.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 1 dated 1-93.

TO-262AA

3 LEAD JEDEC TO-262AA PLASTIC PACKAGE



Lead No. 1	-	Gate
Lead No. 2	-	Drain
Lead No. 3	-	Source
Term. 4 Mounting Flange	-	Drain

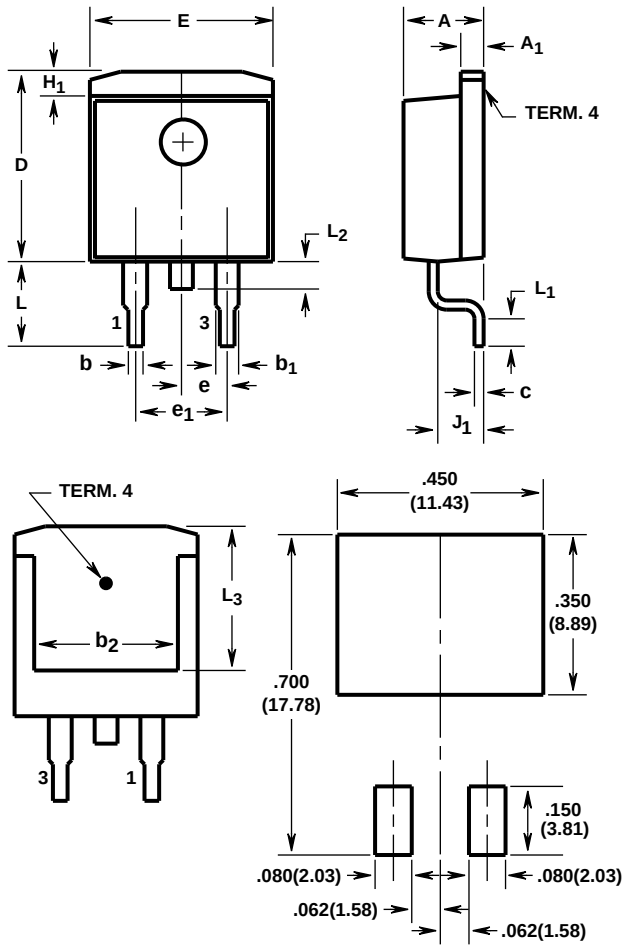
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	3, 4
b	0.030	0.034	0.77	0.86	3, 4
b_1	0.045	0.055	1.15	1.39	3, 4
c	0.018	0.022	0.46	0.55	3, 4
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		5
e_1	0.200 BSC		5.08 BSC		5
H_1	0.045	0.055	1.15	1.39	-
J_1	0.095	0.105	2.42	2.66	6
L	0.530	0.550	13.47	13.97	-
L_1	0.110	0.130	2.80	3.30	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. A of JEDEC TO-262AA outline dated 6-90.
2. Solder finish uncontrolled in this area.
3. Dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder plating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 4 dated 10-95.

TO-263AB

SURFACE MOUNT JEDEC TO-263AB PLASTIC PACKAGE



MINIMUM PAD SIZE RECOMMENDED FOR SURFACE-MOUNTED APPLICATIONS

Lead No. 1	-	Gate
Lead No. 3	-	Source
Term. 4 Mounting Flange	-	Drain

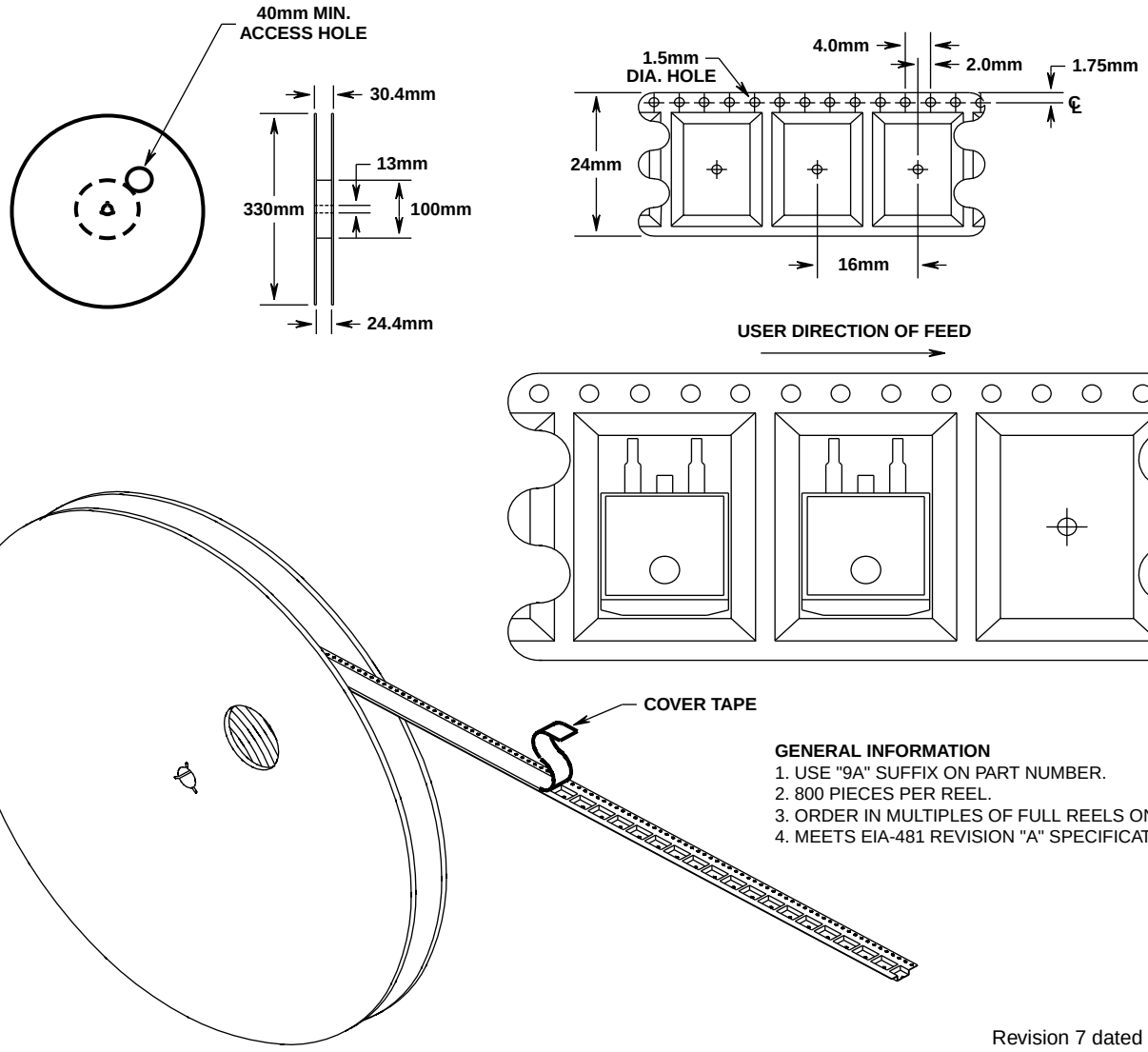
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	4, 5
b	0.030	0.034	0.77	0.86	4, 5
b_1	0.045	0.055	1.15	1.39	4, 5
b_2	0.310	-	7.88	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		7
e_1	0.200 BSC		5.08 BSC		7
H_1	0.045	0.055	1.15	1.39	-
J_1	0.095	0.105	2.42	2.66	-
L	0.175	0.195	4.45	4.95	-
L_1	0.090	0.110	2.29	2.79	4, 6
L_2	0.050	0.070	1.27	1.77	3
L_3	0.315	-	8.01	-	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-263AB outline dated 2-92.
2. L_3 and b_2 dimensions established a minimum mounting surface for terminal 4.
3. Solder finish uncontrolled in this area.
4. Dimension (without solder).
5. Add typically 0.002 inches (0.05mm) for solder plating.
6. L_1 is the terminal length for soldering.
7. Position of lead to be measured 0.120 inches (3.05mm) from bottom of dimension D.
8. Controlling dimension: Inch.
9. Revision 7 dated 10-95.

TO-263AB

24mm TAPE AND REEL



GENERAL INFORMATION

1. USE "9A" SUFFIX ON PART NUMBER.
2. 800 PIECES PER REEL.
3. ORDER IN MULTIPLES OF FULL REELS ONLY.
4. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

Revision 7 dated 10-95

All Harris Semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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