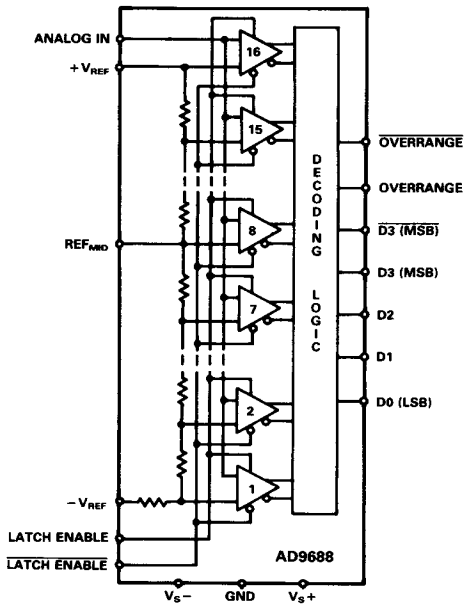
High Speed 4-Bit Monolithic ADC

AD9688

FEATURES
200MSPS Encode Rate
7-Bit Differential Linearity
Bipolar Input Range
Wide Input Range −2.7V to +3.0V

APPLICATIONS
Digital Radio
Electronic Warfare (ECM, ECCM, ESM)
Radar Guidance Digitizers
Smart Munitions

AD9688 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9688 is a 4-bit, high speed, analog-to-digital converter with ECL compatible outputs. The AD9688 is a pin compatible alternate source for the AM6688. The AD9688 is fabricated in a high-performance, bipolar process which allows full Nyquist operation up to 200MSPS encode rates.

The AD9688 provides 7-bit linearity (0.0625LSB for a 4-bit device) which, when combined with the wide input range, allows several AD9688s to be stacked for higher resolutions. Stacking is aided by the overrange output terminals which can be used to drive decoding logic.

The sixteen high speed input comparators will track input signals up to 200MHz. The comparator sampling is controlled by the differential Latch Enable input. The Latch Enable is designed to be driven by 10K or 100K ECL logic families. The outputs of the AD9688 are open emitter terminals (10K and 10KH compatible) requiring pull-down resistors.

The AD9688 is offered as both an industrial temperature range device −25°C to +85°C, and as an extended temperature range device, −55°C to +125°C. Both versions are available packaged in an 18-pin ceramic DIP. The extended temperature range device is also available in a ceramic LCC package.

ORDERING INFORMATION

Device	Linearity	Temperature Range	Description	Package Options*
AD9688BQ	0.125LSB	−25°C to +85°C	18-Pin Cerdip, Industrial	Q-18
AD9688TE	0.125LSB	−55°C to +125°C	20-Pin LCC, Extended Temperature	E-20A
AD9688TQ	0.125LSB	−55°C to +125°C	18-Pin Cerdip, Extended Temperature	Q-18

*See Section 14 for package outline information.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±7V
Analog-to-Digital Ground Voltage Differential 0.5V
Analog Input Voltages
(V_{IN}, $+V_{REF}$, V_{REF}, REF_{MID})[2] . . . . . −4.0 to 4.0V
Differential Reference Voltage ($+V_{REF}$ to $-V_{REF}$)[3] . . . 7.0V
Reference Midpoint Current . . . . . ±4mA
LATCH ENABLE Input Voltages . . . . . −5.2V to 0V
Differential LATCH ENABLE Voltage 5.2V
Digital Output Current 20mA
Power Dissipation (+25°C Free Air)[4] 1.3W
Operating Temperature Range
AD9688BQ . . . . . −25°C to +85°C
AD9688TE/TQ . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature . . . . . +175°C
Lead Soldering Temperature (10sec) . . . . . +300°C

ELECTRICAL CHARACTERISTICS

(Supply Voltages = −5.2V and +5.0V, Differential Reference Voltage = 2.56V, unless otherwise stated)

Parameter	Temp	AD9688BQ Min	AD9688BQ Typ	AD9688BQ Max	AD9688TE/TQ Min	AD9688TE/TQ Typ	AD9688TE/TQ Max	Units
RESOLUTION		4			4			Bits
DC ACCURACY								
Differential Linearity	+25°C		0.04	0.0625		0.04	0.0625	LSB
	Full			0.125			0.125	LSB
Integral Linearity	+25°C		0.055	0.0625		0.055	0.0625	LSB
	Full			0.0625			0.0625	LSB
Transition Error Voltage	Full			10			10	mV
No Missing Codes	Full		GUARANTEED			GUARANTEED		
INITIAL OFFSET ERROR								
Top of Reference Ladder	+25°C		13.0	20.0		13.0	20.0	mV
	Full			25.0			25.0	mV
Bottom of Reference Ladder	+25°C		5.0	10.0		5.0	10.0	mV
	Full			15.0			15.0	mV
Offset Drift Coefficient	Full		30			30		µV/°C
ANALOG INPUT								
Input Voltage Range	Full		−2.7, +3.3			−2.7, +3.3		V
Input Bias Current[5]	+25°C		125	175		125	175	µA
	Full			230			230	µA
Input Resistance	+25°C		40			40		kΩ
Input Capacitance	+25°C		10.3	13.0		10.3	13.0	pF
Full Power Bandwidth[6]	+25°C		100			100		MHz
REFERENCE INPUT[2,3]								
Reference Ladder Resistance	+25°C	280	350	420	280	350	420	Ω
Ladder Temperature Coefficient	Full		0.75			0.75		Ω/°C
Reference Input Bandwidth	+25°C		20			20		MHz
DYNAMIC PERFORMANCE[7]								
Conversion Rate	+25°C	175	200		175	200		MHz
Conversion Time	+25°C		5.0	5.7		5.0	5.7	ns
Minimum Output Hold Time (t_{OH})[8]	+25°C	3.0	3.9		3.0	3.9		ns
Output Delay (t_{PD})[9]	+25°C		6.0	6.5		6.0	6.5	ns
Analog Hold Time (t_H)	+25°C		0.8			0.8		ns
Analog Setup Time (t_S)	+25°C		1.5			1.5		ns
Transient Response[10]	+25°C		3.7			3.7		ns
Overvoltage Recovery Time[11]	+25°C		3.9			3.9		ns
Rise Time	+25°C		2.2	3.0		2.2	3.0	ns
Fall Time	+25°C		2.0	3.0		2.0	3.0	ns
Output Time Skew[12]	+25°C		0.6			0.6		ns
Dynamic Linearity	+25°C		0.1			0.1		LSB

Parameter	Temp	AD9688BQ Min	AD9688BQ Typ	AD9688BQ Max	AD9688TE/TQ Min	AD9688TE/TQ Typ	AD9688TE/TQ Max	Units
LATCH ENABLE INPUT[13]								
Logic "1" Voltage	Full			−1.1			−1.1	V
Logic "0" Voltage	Full	−1.5			−1.5			V
Logic "1" Current	Full			75			75	μA
Logic "0" Current	Full			2			2	μA
Input Capacitance	+25°C		3.5	4.0		3.5	4.0	pF
Latch Enable Pulse Width (LATCHED)	+25°C	3.5	2.8		3.5	2.8		ns
Latch Enable Pulse Width (SAMPLED)	+25°C	2.2	1.3		2.2	1.3		ns
DIGITAL OUTPUTS[7]								
Logic "1" Voltage	Full	−1.1			−1.1			V
Logic "0" Voltage	Full			−1.5			−1.5	V
POWER SUPPLY[14]								
Positive Supply Current (+5.0V)	+25°C		65	70		65	70	mA
	Full			75			75	mA
Negative Supply Current (−5.2V)	+25°C		71	80		71	80	mA
	Full			85			85	mA
Nominal Power Dissipation	+25°C		694			694		mW
Reference Ladder Dissipation	+25°C		19			19		mW
Power Supply Rejection Ratio[15]	+25°C		6.5	10		6.5	10	mV/V

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

[2]Under normal operating conditions, the analog input voltages should not exceed −3.3V to +2.7V.

[3]Under normal operating conditions, the differential reference voltage may range from 0.16V to 6.0V; $+V_{REF} \geq -V_{REF}$.

[4]Typical thermal impedance . . .

18-Pin Ceramic $\theta_{JA} = 75°C/W; \theta_{JC} = 19°C/W$

20-Pin LCC $\theta_{JA} = 80°C/W; \theta_{JC} = 23°C/W$

[5]Sample mode with $A_{IN} = +V_{REF}$.

[6]Determined by no missing codes in the reconstructed output.

[7]Outputs terminated with 100Ω resistors to −2.0V.

[8]Previous output data will remain valid for specified time after the leading edge of the LATCH ENABLE.

[9]Measured from trailing edge of LATCH ENABLE pulse to data out.

[10]For full-scale step input, 6-bit accuracy is attained in specified time.

[11]Recovers to 6-bit accuracy in specified time, after 150% full-scale input overvoltage.

[12]Output time skew includes high-to-low and low-to-high transitions as well as bit-to-bit skew differences.

[13]LATCH ENABLE and $\overline{\text{LATCH ENABLE}}$ are differential inputs which must be driven concurrently. ECL inputs within the specified ranges are guaranteed to produce normal switching.

[14]Supply voltages should remain stable within ±5% for normal operation.

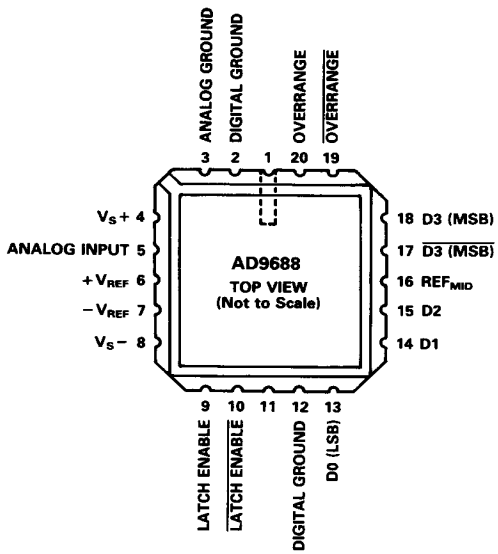
[15]Measured at +5.0V ±5% and −5.2V ±5%.

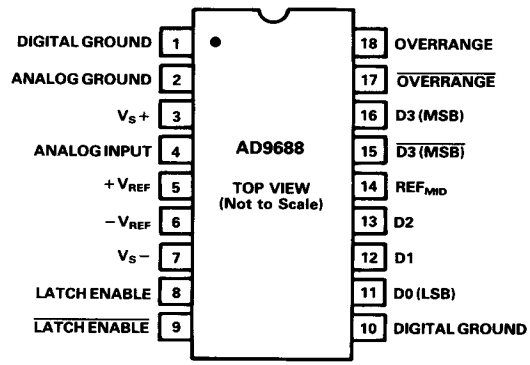
Specifications subject to change without notice.

FUNCTIONAL DESCRIPTION

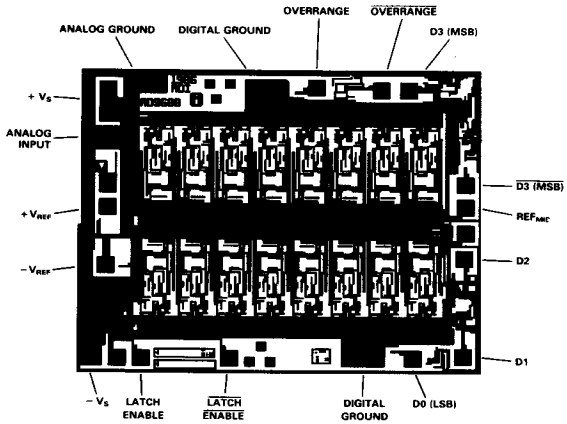
PIN NAME	DESCRIPTION
DIGITAL GROUND	– One of two digital ground returns. All grounds should be connected together near the AD9688.
ANALOG GROUND	– Analog ground return. All grounds should be connected together near the AD9688.
V_S+	– Positive supply terminal, nominally +5.0V.
ANALOG INPUT	– Analog input terminal.
$+V_{REF}$	– Most positive reference voltage for the internal resistor ladder.
$-V_{REF}$	– Most negative reference voltage for the internal resistor ladder.
V_S-	– Negative supply terminal, nominally −5.2V.
LATCH ENABLE	– Noninverting input of differential latch enable input. In the "latch" mode, logic HIGH, the output data reflects the analog input level just prior to the "latched" state. In the "sample" mode, logic LOW, the output data will attempt to track the analog input. The LATCH ENABLE must be driven in conjunction with the $\overline{\text{LATCH ENABLE}}$ input.
$\overline{\text{LATCH ENABLE}}$	– Inverting input of differential latch enable input. In the "latch" mode, logic LOW, the output data reflects the analog input level just prior to the "latched" state. In the "sample" mode logic HIGH, the output data will attempt to track the analog input. The $\overline{\text{LATCH ENABLE}}$ must be driven in conjunction with the LATCH ENABLE input.
DIGITAL GROUND	– One of two digital ground returns. All grounds should be connected together near the AD9688.
D0 (LSB)	– One of four digital outputs. D0 (LSB) is the least significant bit of the digital output word.
D1	– One of four digital outputs.
D2	– One of four digital outputs.
REF_{MID}	– The midpoint tap on the internal reference ladder.
$\overline{\text{D3 (MSB)}}$	– One of four digital outputs. $\overline{\text{D3 (MSB)}}$ is the inverted, most significant bit of the digital output word.
D3 (MSB)	– One of four digital outputs. D3 (MSB) is the most significant bit of the digital output word.
$\overline{\text{OVERRANGE}}$	– Inverted overrange data output. Logic LOW indicates an input voltage overrange ($V_{IN} > +V_{REF}$). All other digital outputs return to zero (logic LOW) during overrange conditions.
OVERRANGE	– Overrange data output. Logic HIGH indicates an input voltage overrange ($V_{IN} > +V_{REF}$). All other digital outputs return to zero (logic LOW) during overrange conditions.

PIN CONFIGURATIONS



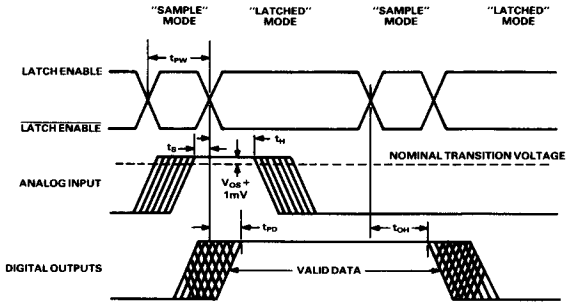


DIE LAYOUT AND MECHANICAL INFORMATION



Die Dimensions	118.5 × 96 × 16 (± 2) mils
Pad Dimensions	4 × 4 mils
Metalization	
1st Level	Copper-Aluminum Alloy
2nd Level	Aluminum
Backing	None
Substrate Potential	$-V_S$
Passivation	Oxynitride
Die Attach	Gold Eutectic
Bond Wire	1.25 mil, Aluminum; Ultrasonic Bonding or 1 mil, Gold; Gold Ball Bonding

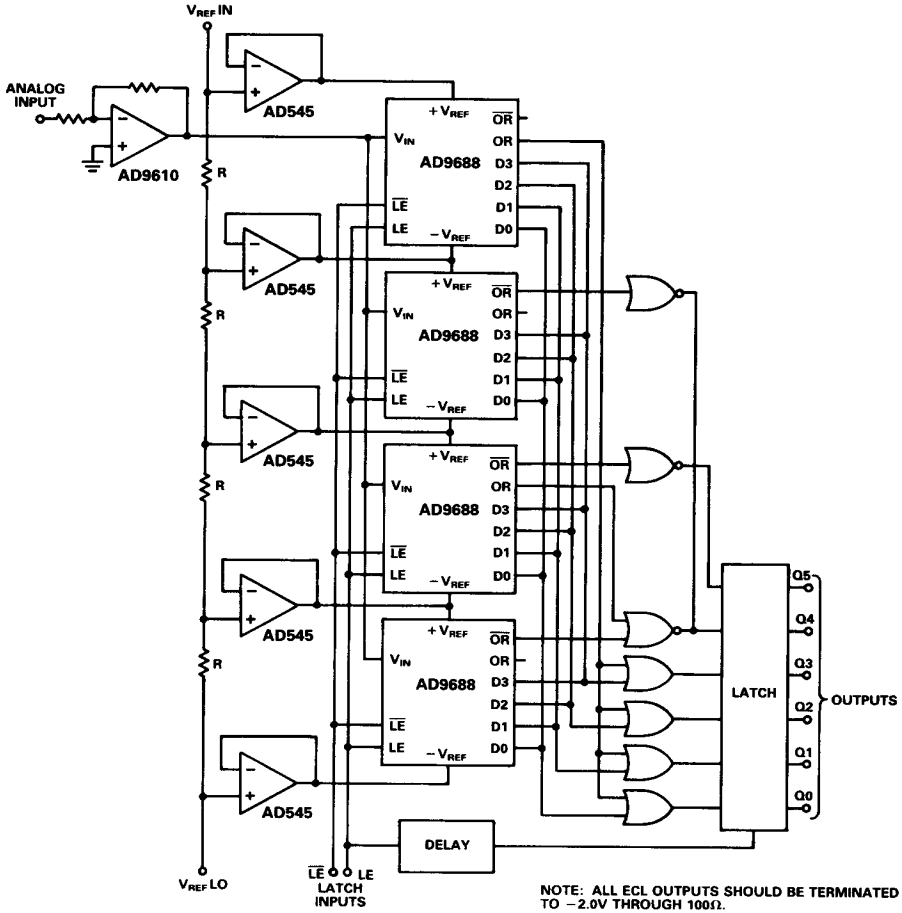
SYSTEM TIMING DIAGRAM



t_{PW}	–	Minimum Sample Pulse Width
t_S	–	Minimum Setup Time
t_H	–	Minimum Hold Time
t_{PD}	–	Maximum Output Propagation Delay
t_{OH}	–	Minimum Output Hold Time
V_{OS}	–	Offset Voltage

NOTE: Comparator outputs are unlatched during "sampling" period. The output may become invalid during this interval as it attempts to track the input signal.

TYPICAL APPLICATION



GENERAL INFORMATION

The AD9688 is a high speed device. The 200MSPS encode rate and analog input frequencies which can reach 200MHz, demand careful layout practice typical of high speed circuit design. One of the most important aspects of any AD9688 design is an effective low impedance ground plane. Special attention should be paid to the actual AD9688 ground connections, particularly if sockets must be used.

The internal reference ladder should be properly biased with some form of low-impedance driving source. This becomes especially important if several AD9688s are stacked for higher resolution. Special transfer functions can be realized when several AD9688s are stacked and the resistor tap point voltages are skewed to approximate the desired response curve.

The AD9688 LATCH ENABLE inputs are differential and must be driven with complementary latch signals. Output stability in the "sampling" mode can be adversely affected by LATCH ENABLE signal quality and precision. The effects of a poor quality waveform can be partially compensated for by adjusting either the average signal value or overall waveform duty cycle.

Best performance will be achieved through the use of proper ECL terminations. The open-emitter outputs of the AD9688 are designed to be terminated through 100Ω resistors to −2.0V. If high speed ECL signals must be routed more than a few centimeters, MicroStrip or StripLine techniques may be required to insure proper transition times and prevent output ringing.