

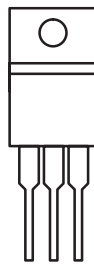
## N-Channel 60-V (D-S), 175 °C MOSFET, Logic Level

PRODUCT SUMMARY		
$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
60	0.022 at $V_{GS} = 10$ V	40
	0.025 at $V_{GS} = 4.5$ V	40

**FEATURES**

- TrenchFET<sup>®</sup> Power MOSFETs
- Maximum Junction Temperature: 175 °C Rated


 Available  
**RoHS\***  
 COMPLIANT

**TO-220AB**


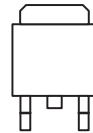
G D S

Top View

SUP40N06-25L

Ordering Information: TO-220AB:

TO-263:

**TO-263**


G D S

Top View

SUB40N06-25L

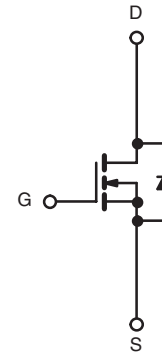
SUP40N06-25L

SUP40N06-25L-E3 (Lead (Pb)-free)

SUB40N06-25L

SUB40N06-25L-E3 (Lead (Pb)-free)

DRAIN connected to TAB



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 175$ °C)	$I_D$	$T_C = 25$ °C	40
		$T_C = 100$ °C	25
Pulsed Drain Current	$I_{DM}$	100	A
Avalanche Current	$I_{AR}$	40	
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	80	mJ
Power Dissipation	$P_D$	$T_C = 25$ °C (TO-220AB and TO-263)	90 <sup>c</sup>
		$T_A = 25$ °C (TO-263) <sup>c</sup>	3.7
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 175	°C

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limit	Unit
Junction-to-Ambient	$R_{thJA}$	PCB Mount (TO-263) <sup>c</sup>	40
		Free Air (TO-220AB)	80
Junction-to-Case	$R_{thJC}$	1.6	°C/W

Notes:

 a. Duty cycle  $\leq 1$  %.

b. See SOA curve for voltage derating.

 c. Surface Mounted on FR4 Board,  $t \leq 10$  sec.

\* Pb containing terminations are not RoHS compliant, exemptions may apply.

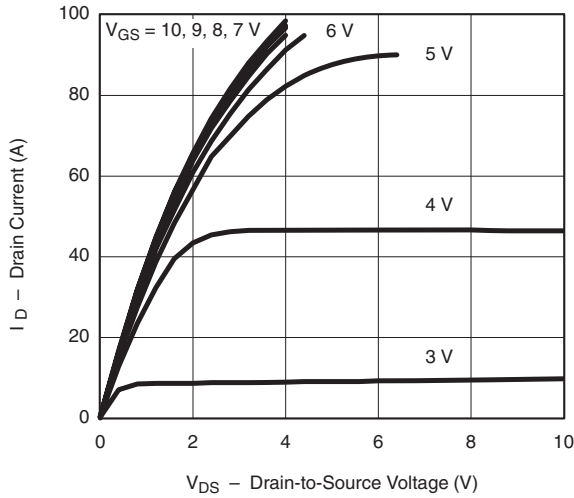
<b>SPECIFICATIONS</b> $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.0	2.0	3.0	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$			50	
		$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}, T_J = 175\text{ }^\circ\text{C}$			150	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} = 5\text{ V}, V_{GS} = 10\text{ V}$	40			A
Drain-Source On-State Resistance <sup>a</sup>	$r_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$			0.022	$\Omega$
		$V_{GS} = 10\text{ V}, I_D = 20\text{ A}, T_J = 125\text{ }^\circ\text{C}$			0.043	
		$V_{GS} = 10\text{ V}, I_D = 20\text{ A}, T_J = 175\text{ }^\circ\text{C}$			0.053	
		$V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$			0.025	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 20\text{ A}$				S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$		1800		$\mu\text{F}$
Output Capacitance	$C_{oss}$			350		
Reverse Transfer Capacitance	$C_{rss}$			100		
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{DS} = 30\text{ V}, V_{GS} = 10\text{ V}, I_D = 40\text{ A}$		40	60	nC
Gate-Source Charge <sup>c</sup>	$Q_{gs}$			9		
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			10		
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = 30\text{ V}, R_L = 0.8\text{ }\Omega$ $I_D \cong 40\text{ A}, V_{GEN} = 10\text{ V}, R_G = 2.5\text{ }\Omega$		10	20	ns
Rise Time <sup>c</sup>	$t_r$			9	20	
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$			28	50	
Fall Time <sup>c</sup>	$t_f$			7	15	
<b>Source-Drain Diode Ratings and Characteristics</b> $T_C = 25\text{ }^\circ\text{C}$ <sup>b</sup>						
Continuous Current	$I_S$				40	A
Pulsed Current	$I_{SM}$				100	
Forward Voltage <sup>a</sup>	$V_{SD}$	$I_F = 40\text{ A}, V_{GS} = 0\text{ V}$		1.0	1.5	V
Reverse Recovery Time	$t_{rr}$	$I_F = 40\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		48	100	ns
Peak Reverse Recovery Charge	$I_{RM(REC)}$			6		A
Reverse Recovery Charge	$Q_{rr}$				0.15	

**Notes:**

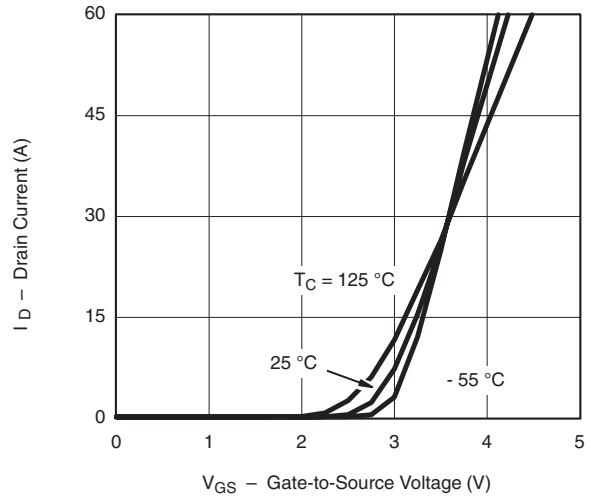
- Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

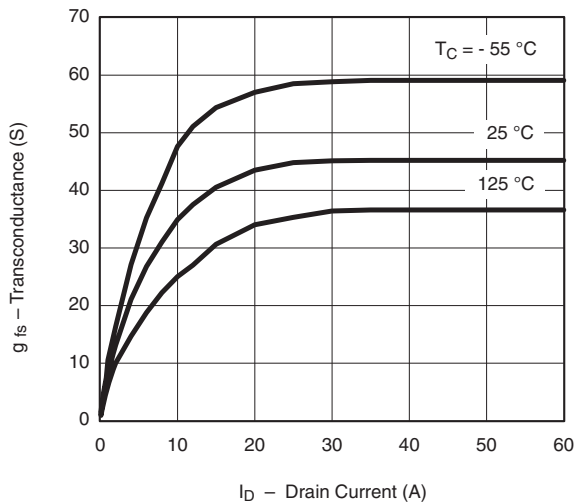
**TYPICAL CHARACTERISTICS** 25 °C unless noted



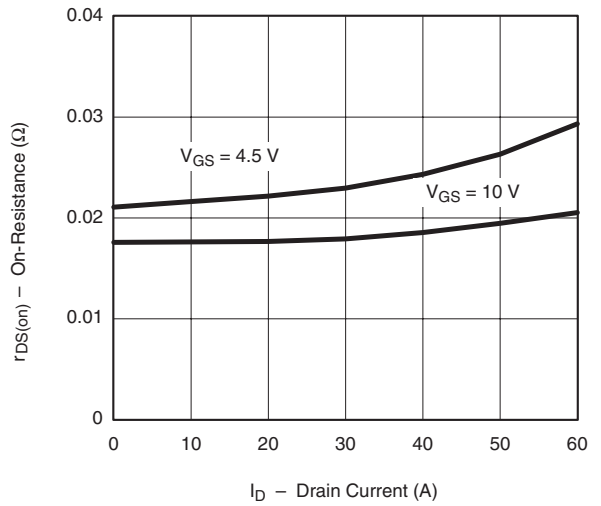
**Output Characteristics**



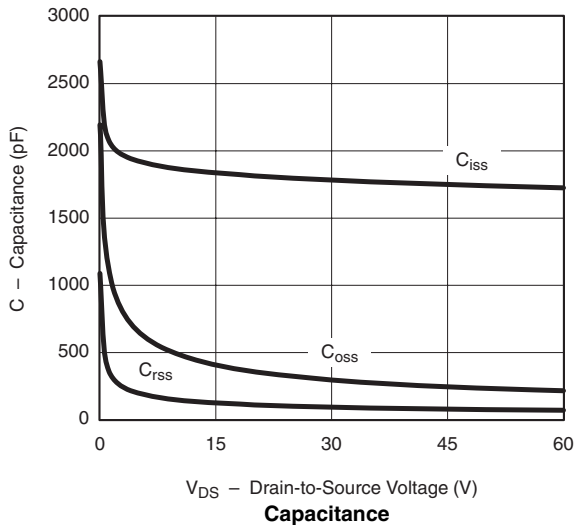
**Transfer Characteristics**



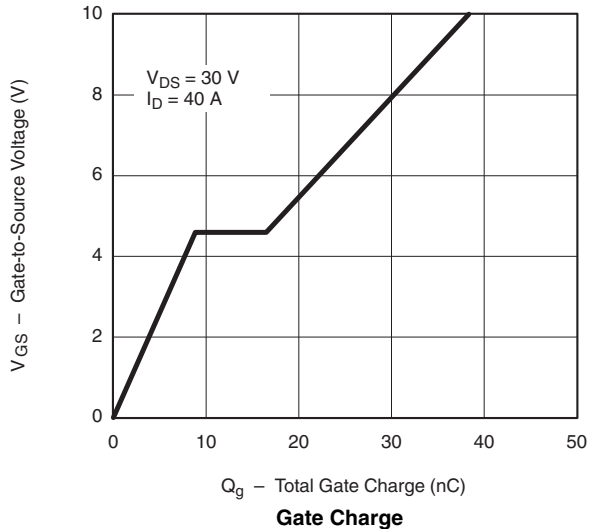
**Transconductance**



**On-Resistance vs. Drain Current**

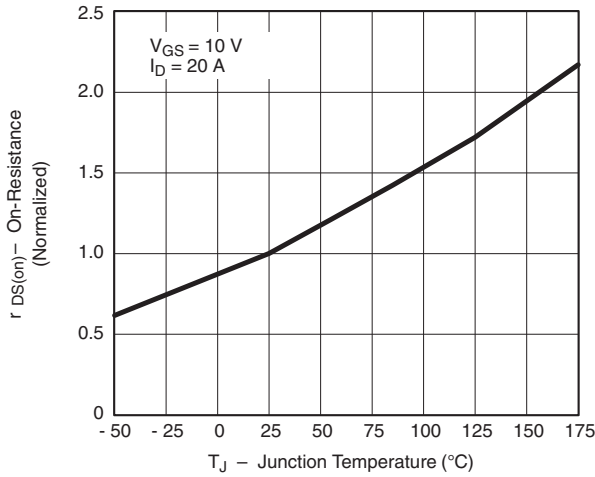


**Capacitance**

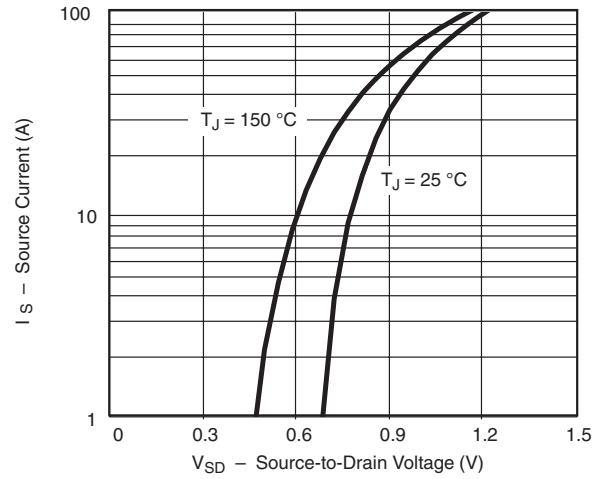


**Gate Charge**

**TYPICAL CHARACTERISTICS** 25 °C unless noted

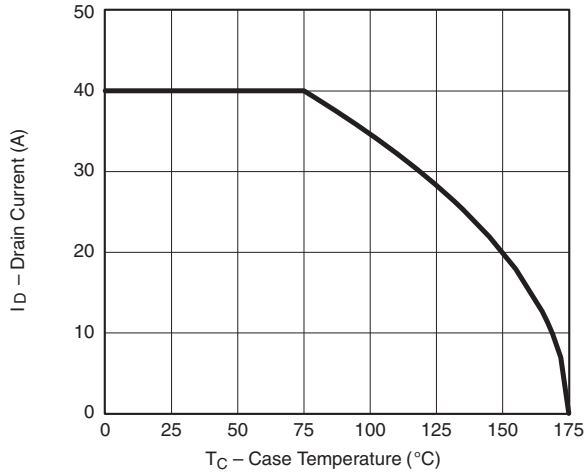


**On-Resistance vs. Junction Temperature**

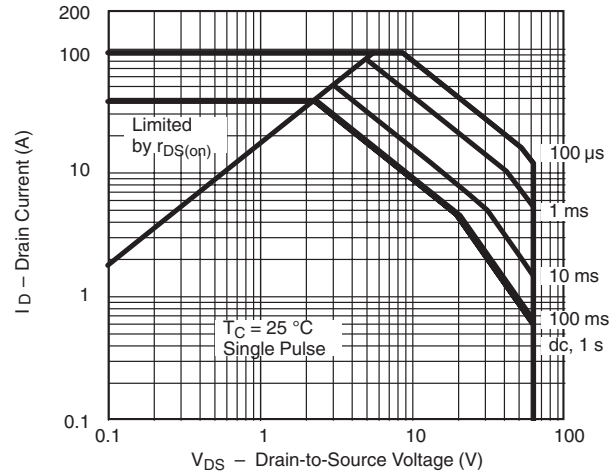


**Source-Drain Diode Forward Voltage**

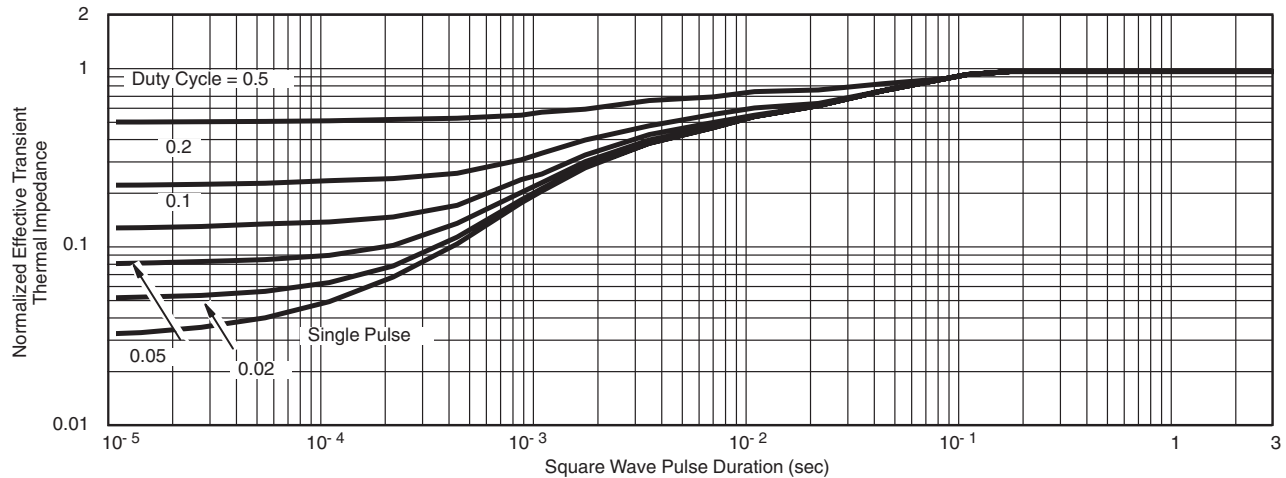
**THERMAL RATINGS**



**Drain Current vs. Case Temperature**



**Safe Operating Area**



**Normalized Thermal Transient Impedance, Junction-to-Case**

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