NIF5002N

Preferred Device

Self-Protected FET with Temperature and Current Limit

42 V, 2.0 A, Single N−Channel, SOT−223

HDPlus™ devices are an advanced series of power MOSFETs which utilize ON Semiconductors latest MOSFET technology process to achieve the lowest possible on−resistance per silicon area while incorporating smart features. Integrated thermal and current limits work together to provide short circuit protection. The devices feature an integrated Drain−to−Gate Clamp that enables them to withstand high energy in the avalanche mode. The Clamp also provides additional safety margin against unexpected voltage transients. Electrostatic Discharge (ESD) protection is provided by an integrated Gate−to−Source Clamp.

Features

- Current Limitation
- Thermal Shutdown with Automatic Restart
- Short Circuit Protection
- I_{DSS} Specified at Elevated Temperature
- Avalanche Energy Specified
- Slew Rate Control for Low Noise Switching
- Overvoltage Clamped Protection

Applications

- Lighting
- Solenoids
- Small Motors

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage Internally Clamped	V_{DSS}	42	V
Drain−to−Gate Voltage Internally Clamped (R_G = 1.0 MΩ)	V_{DGR}	42	V
Gate−to−Source Voltage	V_{GS}	±14	V
Continuous Drain Current	I_D	Internally Limited	
Power Dissipation @ T_A = 25°C (Note 1) @ T_A = 25°C (Note 2) @ T_T = 25°C (Note 3)	P_D	1.1 1.7 8.9	W
Operating Junction and Storage Temperature	T_J, T_{stg}	−55 to 150	°C
Single Pulse Drain−to−Source Avalanche Energy (V_{DD} = 32 V, V_G = 5.0 V, I_{PK} = 1.0 A, L = 300 mH, $R_{G(ext)}$ = 25 Ω)	E_{AS}	150	mJ

THERMAL RESISTANCE RATINGS

Rating	Symbol	Value	Unit
Junction−to−Ambient − Steady State (Note 1) Junction−to−Ambient − Steady State (Note 2) Junction−to−Tab − Steady State (Note 3)	$R_{\theta JA}$ $R_{\theta JA}$ $R_{\theta JT}$	114 72 14	°C/W

1. Surface−mounted onto min pad FR4 PCB, (2 oz. Cu, 0.06″ thick).
2. Surface−mounted onto 2″ sq. FR4 board (1″ sq., 1 oz. Cu, 0.06″ thick).
3. Surface−mounted onto min pad FR4 PCB, (2 oz. Cu, 0.06″ thick).

ON Semiconductor®

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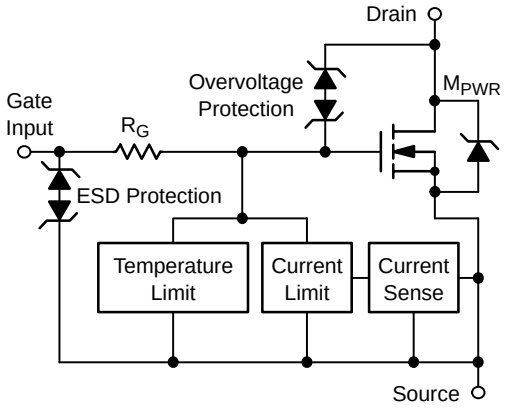
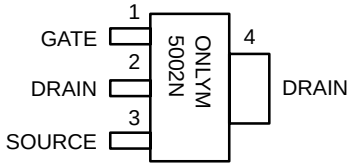
$V_{(BR)DSS}$ (Clamped)	$R_{DS(ON)}$ TYP	I_D MAX
42 V	165 mΩ @ 10 V	2.0 A*

*Max current limit value is dependent on input condition.



SOT−223
CASE 318E
Style 3

MARKING DIAGRAM



(Top View)

5002N = Specific Device Code
L = Location Code
YM = Year, Month

ORDERING INFORMATION

Device	Package	Shipping†
NIF5002NT1	SOT−223	1000/Tape & Reel
NIF5002NT3	SOT−223	4000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage (Note 4)	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 mA	T_J = 25°C	42	46	55	V
			T_J = 150°C	40	45	55	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 32 V	T_J = 25°C		0.25	4.0	μA
			T_J = 150°C		1.1	20	
Gate Input Current	I_{GSSF}	V_{DS} = 0 V, V_{GS} = 5.0 V			50	100	μA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 150 μA		1.3	1.8	2.2	V
Gate Threshold Temperature Coefficient	$V_{GS(th)}/T_J$				4.0	6.0	−mV/°C
Static Drain−to−Source On−Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 1.7 A	T_J = 25°C		165	200	mΩ
			T_J = 150°C		305	400	
		V_{GS} = 5.0 V, I_D = 1.7 A	T_J = 25°C		195	230	
			T_J = 150°C		360	460	
		V_{GS} = 5.0 V, I_D = 0.5 A	T_J = 25°C		190	230	
			T_J = 150°C		350	460	
Source−Drain Forward On Voltage	V_{SD}	V_{GS} = 0 V, I_S = 7.0 A			1.0		V
SWITCHING CHARACTERISTICS							
Turn−on Time	$t_{d(on)}$	V_{GS} = 10 V, V_{DD} = 12 V, I_D = 2.5 A, R_L = 4.7 Ω, (10% V_{in} to 90% I_D)			20	30	μs
Turn−off Time	$t_{d(off)}$				65	100	
Slew Rate On	dV_{DS}/dt_{on}	R_L = 4.7 Ω, V_{in} = 0 to 10 V, V_{DD} = 12 V, 70% to 50%			1.2		V/μs
Slew−Rate Off	dV_{DS}/dt_{off}	R_L = 4.7 Ω, V_{in} = 0 to 10 V, V_{DD} = 12 V, 50% to 70%			0.5		
SELF PROTECTION CHARACTERISTICS (T_J = 25°C unless otherwise noted) (Note 5)							
Current Limit	I_{LIM}	V_{DS} = 10 V, V_{GS} = 5.0 V	T_J = 25°C	3.1	4.7	6.3	A
			T_J = 150°C	2.0	3.2	4.3	
		V_{DS} = 10 V, V_{GS} = 10 V	T_J = 25°C	3.8	5.7	7.6	
			T_J = 150°C	2.8	4.3	5.7	
Temperature Limit (Turn−off)	$T_{LIM(off)}$	V_{GS} = 5.0 V		150	175	200	°C
Temperature Limit (Circuit Reset)	$T_{LIM(on)}$	V_{GS} = 5.0 V		135	160	185	
Temperature Limit (Turn−off)	$T_{LIM(off)}$	V_{GS} = 10 V		150	165	185	
Temperature Limit (Circuit Reset)	$T_{LIM(on)}$	V_{GS} = 10 V		135	150	170	
ESD ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)							
Electro−Static Discharge Capability	ESD	Human Body Model (HBM)		4000			V
		Machine Model (MM)		400			

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
5. Fault conditions are viewed as beyond the normal operating range of the part.

TYPICAL PERFORMANCE CURVES

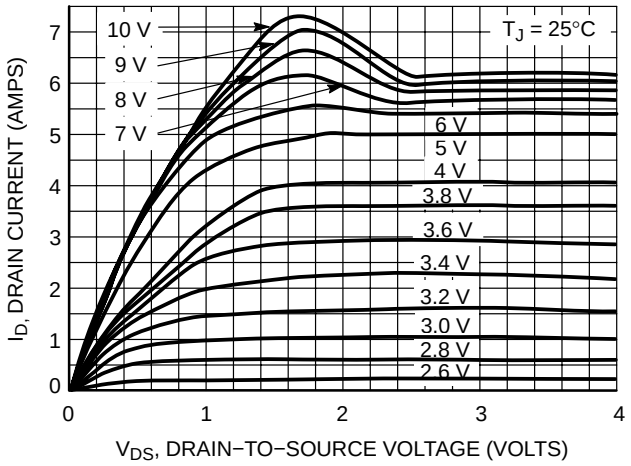


Figure 1. On−Region Characteristics

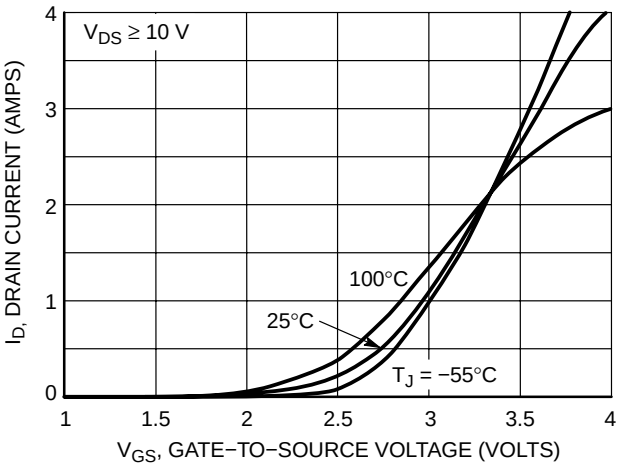


Figure 2. Transfer Characteristics

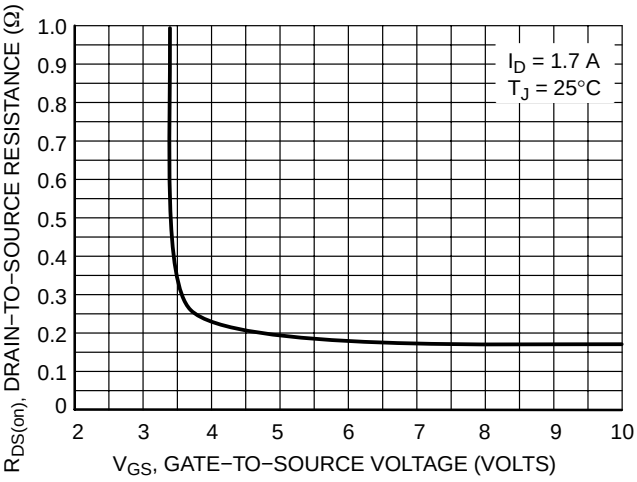


Figure 3. On−Resistance vs. Gate−to−Source Voltage

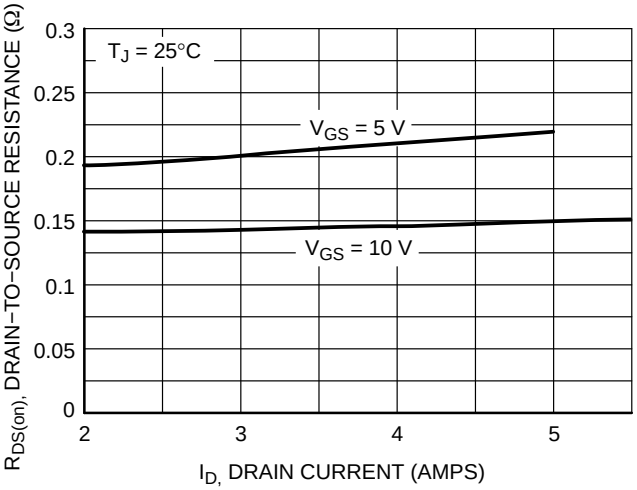


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

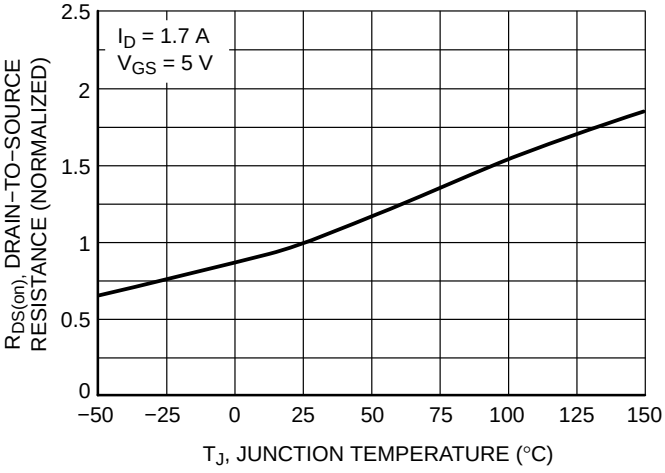


Figure 5. On−Resistance Variation with Temperature

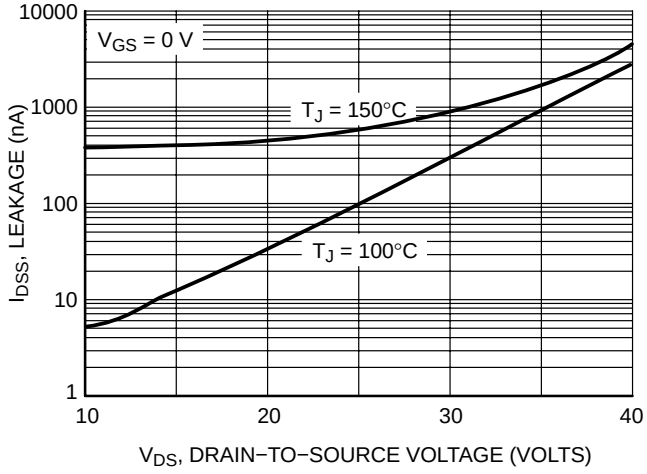


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

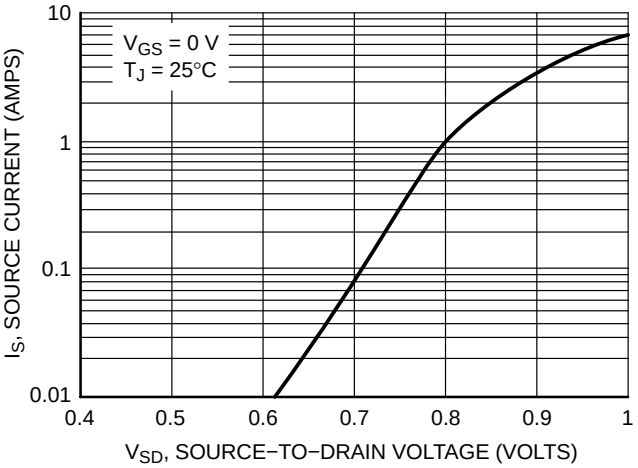


Figure 7. Diode Forward Voltage vs. Current

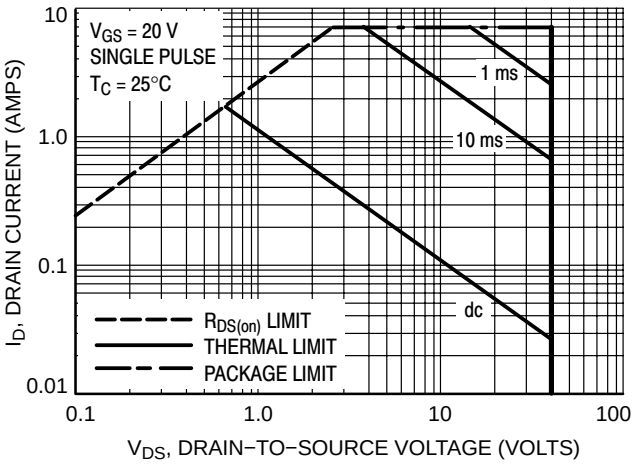


Figure 8. Maximum Rated Forward Biased Safe Operating Area

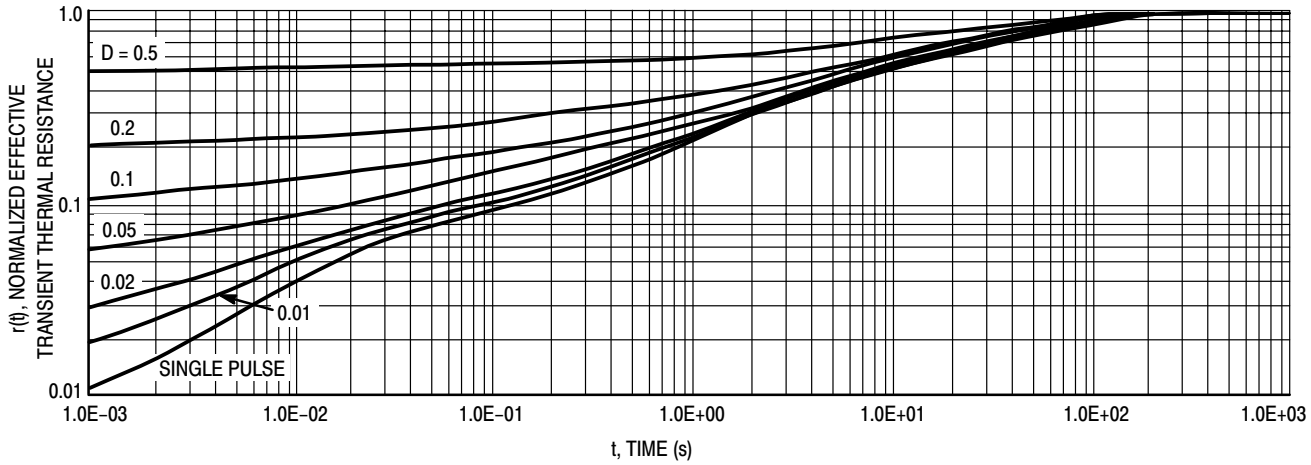
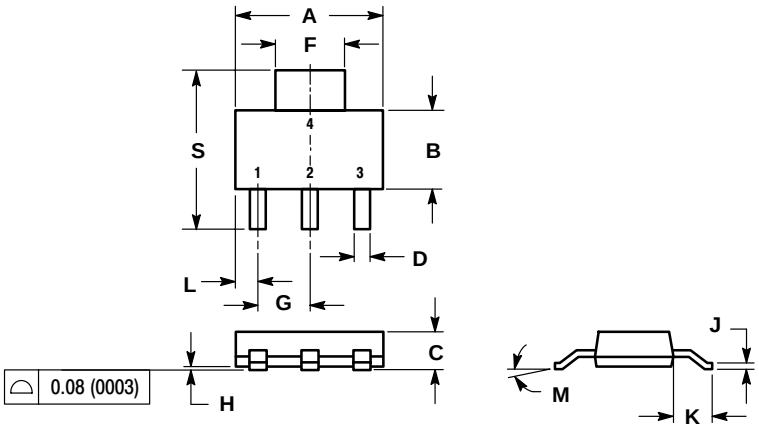


Figure 9. Thermal Response

PACKAGE DIMENSIONS

SOT−223
CASE 318E−04
ISSUE K



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.249	0.263	6.30	6.70
B	0.130	0.145	3.30	3.70
C	0.060	0.068	1.50	1.75
D	0.024	0.035	0.60	0.89
F	0.115	0.126	2.90	3.20
G	0.087	0.094	2.20	2.40
H	0.0008	0.0040	0.020	0.100
J	0.009	0.014	0.24	0.35
K	0.060	0.078	1.50	2.00
L	0.033	0.041	0.85	1.05
M	0 °	10 °	0 °	10 °
S	0.264	0.287	6.70	7.30

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
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