

MTP50P03HDL

Preferred Device

Power MOSFET 50 Amps, 30 Volts, Logic Level P-Channel TO-220

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The energy efficient design also offers a drain-to-source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

Features

- Avalanche Energy Specified
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Pb-Free Package is Available*

MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	30	Vdc
Drain-Gate Voltage ($R_{GS} = 1.0\text{ M}\Omega$)	V_{DGR}	30	Vdc
Gate-Source Voltage - Continuous - Non-Repetitive ($t_p \leq 10\text{ ms}$)	V_{GS} V_{GSM}	± 15 ± 20	Vdc Vpk
Drain Current - Continuous - Continuous @ 100°C - Single Pulse ($t_p \leq 10\ \mu\text{s}$)	I_D I_{DM}	50 31 150	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	125 1.0	W W/ $^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy - Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 25\text{ Vdc}$, $V_{GS} = 5.0\text{ Vdc}$, Peak $I_L = 50\text{ Apk}$, $L = 1.0\text{ mH}$, $R_G = 25\ \Omega$)	E_{AS}	1250	mJ
Thermal Resistance, Junction-to-Case Junction-to-Ambient, when mounted with the minimum recommended pad size	$R_{\theta JC}$ $R_{\theta JA}$	1.0 62.5	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	$^\circ\text{C}$

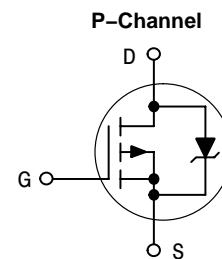
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

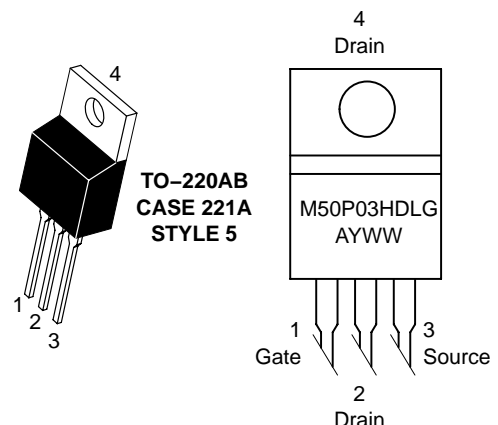


ON Semiconductor®

50 AMPERES, 30 VOLTS
 $R_{DS(on)} = 25\text{ m}\Omega$



MARKING DIAGRAM & PIN ASSIGNMENT



M50P03HDL = Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping
MTP50P03HDL	TO-220AB	50 Units/Rail
MTP50P03HDLG	TO-220AB (Pb-Free)	50 Units/Rail

Preferred devices are recommended choices for future use and best overall value.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 250 μAdc) Temperature Coefficient (Positive)	V _{(BR)DSS}	30	- 26	-	Vdc mV/°C	
Zero Gate Voltage Drain Current (V _{DS} = 30 Vdc, V _{GS} = 0 Vdc) (V _{DS} = 30 Vdc, V _{GS} = 0 Vdc, T _J = 125°C)	I _{DSS}	-	-	1.0 10	μAdc	
Gate-Body Leakage Current (V _{GS} = ± 15 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	-	-	100	nAdc	
ON CHARACTERISTICS (Note 1)						
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 250 μAdc) Threshold Temperature Coefficient (Negative)	V _{GS(th)}	1.0	1.5 4.0	2.0	Vdc mV/°C	
Static Drain-to-Source On-Resistance (V _{GS} = 5.0 Vdc, I _D = 25 Adc)	R _{DS(on)}	-	0.020	0.025	Ω	
Drain-to-Source On-Voltage (V _{GS} = 10 Vdc) (I _D = 50 Adc) (I _D = 25 Adc, T _J = 125°C)	V _{DS(on)}	-	0.83 -	1.5 1.3	Vdc	
Forward Transconductance (V _{DS} = 5.0 Vdc, I _D = 25 Adc)	g _{FS}	15	20	-	mhos	
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V _{DS} = 25 Vdc, V _{GS} = 0 Vdc, f = 1.0 MHz)	C _{ISS}	-	3500	4900	pF
Output Capacitance		C _{OSS}	-	1550	2170	
Transfer Capacitance		C _{RSS}	-	550	770	
SWITCHING CHARACTERISTICS (Note 2)						
Turn-On Delay Time	(V _{DD} = 15 Vdc, I _D = 50 Adc, V _{GS} = 5.0 Vdc, R _G = 2.3 Ω)	t _{d(on)}	-	22	30	ns
Rise Time		t _r	-	340	466	
Turn-Off Delay Time		t _{d(off)}	-	90	117	
Fall Time		t _f	-	218	300	
Gate Charge (See Figure 8)	(V _{DS} = 24 Vdc, I _D = 50 Adc, V _{GS} = 5.0 Vdc)	Q _T	-	74	100	nC
		Q ₁	-	13.6	-	
		Q ₂	-	44.8	-	
		Q ₃	-	35	-	
SOURCE-DRAIN DIODE CHARACTERISTICS						
Forward On-Voltage	(I _S = 50 Adc, V _{GS} = 0 Vdc) (I _S = 50 Adc, V _{GS} = 0 Vdc, T _J = 125°C)	V _{SD}	-	2.39 1.84	3.0	Vdc
Reverse Recovery Time (See Figure 15)		t _{rr}	-	106	-	
Reverse Recovery Stored Charge	(I _S = 50 Adc, V _{GS} = 0 Vdc, di _S /dt = 100 A/μs)	t _a	-	58	-	
		t _b	-	48	-	
		Q _{RR}	-	0.246	-	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L _D	-	3.5 4.5	-	nH	
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)	L _S	-	7.5	-	nH	

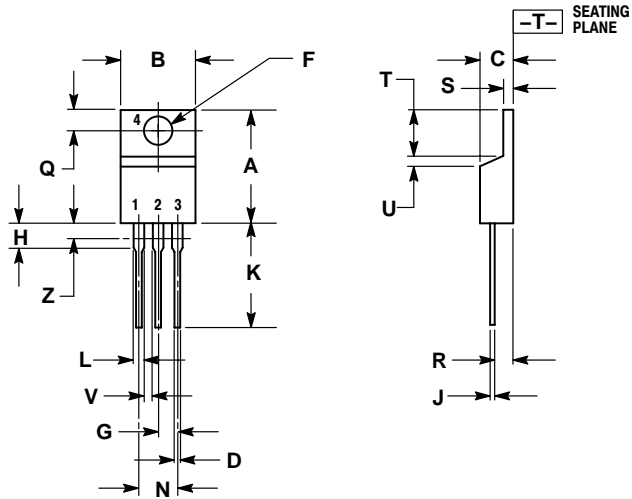
1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.
3. Reflects typical values.

$$C_{pk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$$

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PACKAGE DIMENSIONS

TO-220
CASE 221A-09
ISSUE AB



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.020	0.055	0.508	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 5:

- PIN 1. GATE
- DRAIN
- SOURCE
- DRAIN